Widening the Bottleneck at the Quantum-Classical Interface

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Abstract

Quantum computing's promise to solve complex, uncomputable problems is likely to require systems with billions of qubits. Creating an efficient interface between such a vast number of qubits and classical systems represents an enormous challenge, critical to fulfilling that promise. In this thesis, I demonstrate that the readout and control subsystems comprising this interface can be engineered in new ways that overcome current non-scalable limitations.

Connecting billions of qubits to classical systems demands innovative solutions to address power dissipation, readout and control overhead, and space constraints. These issues stem from the bottleneck in the cryogenic fridge housing the quantum systems, where ultra-low temperature requirements impose space and cooling power limitations. Reducing the per-qubit load is a requirement of scale-up, and while many novel approaches have been proposed [1–18], questions remain on their effect on the qubits themselves.

If future qubits have significantly higher fidelities than those available today, then far fewer are needed to achieve the same level of effectiveness. My first experiment explores this possibility by examining a measurement-only approach to topological states. Topological architectures have long promised qubits far more robust to noise compared to those of today, however engineering challenges have prevented their realisation. A measurement-only approach alleviates some of these challenges, and to validate this idea, a trivial topological state (the Aharonov-Bohm effect) is measured using a dispersive gate sensing (DGS) technique. We find that this state can be read out using DGS, with the measurement speed far surpassing that of conventional transport measurement methods. Applying DGS to other architectures also reduces their per-qubit load, as it eliminates the need for a discrete charge sensor, thereby decreasing the number of connections required for a quantum device.

Billions of qubits will require billions of wires for readout and control, and trying to route them all down a space- and power-limited cryogenic fridge is an exercise in futility. In my second experiment, I examine an alternative approach: generating the control signals locally. By placing control electronics much closer to the qubits (millimeters vs. meters), only a few power and digital lines are needed to connect to the outside world. An open question remains, however, as to the impact of proximally-placed electronics on qubit fidelities. Here, I show that not only is cryo-CMOS capable of performing universal logic operations for spin qubits, it also does so with minimal impact on the fidelities of the qubits themselves. This heralds a new control architecture, based on heterogeneous integration of quantum and classical components.

Together, these solutions constitute part of a broader effort to reduce the cost of scaling quantum systems. By minimizing the number of control and readout lines needed to link quantum and classical systems, we pave the way for rapid scaling of qubits. This is a crucial step in our quest to build practical and useful quantum systems.

Declaration

I certify that to the best of my knowledge, the content of this thesis is my own work and that all the assistance received in preparing this thesis and sources have been acknowledged. This thesis has not been submitted for any degree or other purposes. No content produced by generative AI tools has been used in the preparation of this thesis. This research was supported by an Australian Government Research Training Program (RTP) Scholarship.

Sam Bartee

Included Publications

Chapter 4
Fast Detection of the Aharonov-Bohm Phase with Gate Reflectometry
S. K. Bartee, J. D. S. Witt, S. J. Waddy, B. J. Villis, M. J. Mandra, and D. J. Reilly
In preparation (2024)
Contributions: Fabrication and measurement of devices, analysis and presentation of data, and writing of the manuscript.

Chapter 5
Spin Qubits with Scalable milli-kelvin CMOS Control
S. K. Bartee, W. Gilbert, K. Zuo, K. Das, T. Tanttu, C. H. Yang, N. D. Stuyck, R. Kalra, S. J. Pauka, R. Y. Su, W. H. Lim, S. Serrano, C. C. Escott, F. E. Hudson, K. M. Itoh, A. Laucht, A. S. Dzurak, and D. J. Reilly
In preparation, submitted to Nature (2024)
Contributions: Measurement of devices, analysis and presentation of data, and writing of the manuscript.

In addition to the statements above, in cases where I am not the corresponding author of a published item, permission to include the published material has been granted by the corresponding author.

Sam Bartee

As supervisor for the candidature upon which this thesis is based, I can confirm that the authorship attribution statements above are correct.

David Reilly

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It was six and a half years ago, as an undergraduate, when I first reached out to my supervisor, Professor David Reilly, about starting a PhD. I could not have imagined how far I've come since that point. This thesis is a testament to all those who helped and supported me throughout.

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Expanding our Problem-Solving Toolset

It takes just five questions to reach the limits of our scientific knowledge: ask what a rock is made of and the answer will probably be several types of minerals; then, ask what those minerals are made from, and you'll get atoms like carbon, potassium, and sodium; ask what are atoms are made of and you'll get protons, neutrons, and electrons; once more about the components of protons, neutrons, and electrons, and you'll encounter terms like up, down, strange, and charmed quarks; and finally, ask again and scientists will give you all sorts of explanations that are rife with disagreement, plus a lot of "I don't know." It's at this point where the pursuit of new knowledge begins.

How do we widen the bottleneck at the quantum-classical interface?
Where does this bottleneck come from?
What costs are there to implementing certain solutions?
How do solutions differ for various architectures?
Is there a fundamental limit to any implementation?

The relentless drive to answer "I don't know" has lead to the discovery of wonderfully weird and counter-intuitive explanations: time passing faster on mountain tops than at sea level, particles changing their behavior depending on whether you look at them, liquids climbing up the walls of a cup to drain out, and the transmutation of elements into other elements. This quest has compelled us to build better tools, which are then used to answer even more questions. It's hard to categorize stars without a telescope. It's even harder to observe time dilation with just a sundial, rather than with an atomic clock. One of the best tools we've ever invented – the computer – has enabled an

unparalleled explosion of scientific breakthroughs. In fact, almost every single scientific discovery of the last century has, in one form or another, been aided by the advent of the computer. Yet despite this century of continuous improvement, we're encountering ever more problems that are immensely difficult for computers to solve. Ask a computer to simulate a simple quantum system, for example, and it may take 100 weeks to do so. Add a bit more onto the system, and suddenly it will take 100 years. The fundamental bit-wise approach that has remained unchanged since the Second World War is the wrong tool for the job.

A quantum computer is a different tool. It leverages the power of quantum mechanics to transform bits into *qubits*, which is a fundamentally novel approach to unlock new efficiencies. An entire class of problems, previously 'intractable' to classical systems (solvable, but realistically unattainable) can be efficiently solved using quantum systems. Does this mean quantum computers will replace classical systems? Likely not, there are too many things that classical computers are *really* good at, that quantum systems may never do better. Instead, quantum systems will serve as part of the larger computing stack, useful in contexts where it makes sense to trade-off speed for accuracy. This limits the subset of problems quantum systems are well-suited for to those that (a) do not need much data input and (b) demand greater accuracy than classical systems can provide. Many of these reside within the quantum realm themselves: chemistry and material science are likely two areas quantum computers are positioned to transform [19]. And yet, until we are able to get a truly useful quantum computer into the hands of users, we don't really know what the killer applications might be.

The unique properties quantum computers use to operate also pose very serious challenges. Building a functional quantum computer is a monumental task requiring the fusion of physics and computer science, two intellectual communities that are just beginning to seriously work together. Understanding the physical dynamics of a system, efficient error correction, and higher level algorithms is only possible with input from both fields. While this thesis is primarily about the field of physics, I believe it's important to provide motivation both from both standpoints. For this reason, the following two sections present an overview of complexity theory and quantum computing. Neither is comprehensive and there are textbooks that cover the subject much more rigorously, such as *Computational Complexity* [20] and *Quantum Computation and Quantum Information* [21].

1.1 Complexity Theory

A branch of theoretical computer science, complexity theory sorts problems into 'classes' that depend on the time and space required to solve them. Much like a zoo, where you'll find mammals and reptiles in one section, and creepy crawlies in another, any particular problem belongs somewhere in the Complexity Zoo, which describes a vast network of overlapping complexity classes [22]. For example, a problem belongs in the *polynomial-time* complexity class P if the answer is found within n^k steps, where k is a non-negative constant and n is input size of the problem. Algorithms used for sorting fall within this category. Certain others are not solvable within polynomial time, but when provided a solution can be checked and verified within polynomial time. These belong to the *nondeterministic polynomial-time* class NP, and the travelling salesman problem is a good example of this.[1] Many more don't belong to either, taking an exponential amount of time to solve and verify.

John Gill introduced the bounded-error probabilistic polynomial-time class BPP, meant to encompass problems solvable in polynomial time with a probability of at least 2/3 of finding the correct answer using probabilistic methods [24].[2] A quantum computer extends this, capable of solving problems of class BQP, or Bounded-Error Quantum Polynomial-Time. We know that $\mathsf{BPP} \subseteq \mathsf{BQP}$, and we know certain problems that belong to this group, including Shor's algorithm [26], Grover's algorithm [27]. Given that quantum computers are in their infancy, just like in the 1940's with classical computers, many previously intractable problems we are yet to discover.

Intractability in classical systems is not a matter just adding more transistors, more RAM and higher clock speed. Despite the promise of advancing into exaflop territory, at some point we run up against the exponential wall. Trying to simulate a quantum computer, for example, requires 2^n amplitudes for n qubits, and operations on n qubits requires a unitary matrix of size $2^n \times 2^n$. That means that we would need upwards of 1 PB of RAM for just 50 qubits, and 100 qubits well exceeds the total data computers have ever produced. Practically speaking, many BQP class problems will only be solved on the advent of a fully realised quantum computer.

[1] The relationship between P and NP has been studied extensively [23], and the intermediate area between the two is of great interest for quantum computing researchers.

[2] It is believed that $\mathsf{P} = \mathsf{BPP}$ [25] but at the very least we know $\mathsf{P} \subseteq \mathsf{BPP}$.

1.2 Quantum Logic

The fundamental building block of a quantum computer is a *qubit*. Qubits in some ways are very much like bits, designed as two-level systems, but they exhibit certain behaviors that make quantum systems an exciting computational tool. If we denote bit systems as the two states $|0\rangle$ and $|1\rangle$:

$$|0\rangle = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \; |1\rangle = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{1.1}$$

Then a qubit can be represented by the equation

$$|\psi\rangle = \alpha\,|0\rangle + \beta|1\rangle = \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{1.2}$$

where the amount of $|0\rangle$-ness or $|1\rangle$-ness is dependent on the strength of the probability $|\alpha^2|$ and $|\beta^2|$ respectively. α and β are complex numbers called amplitudes, and satisfy $|\alpha^2| + |\beta^2| = 1$.

The state of a qubit can be visualized on a Bloch sphere, a sphere of unit radius where the qubit state exists somewhere on the surface.

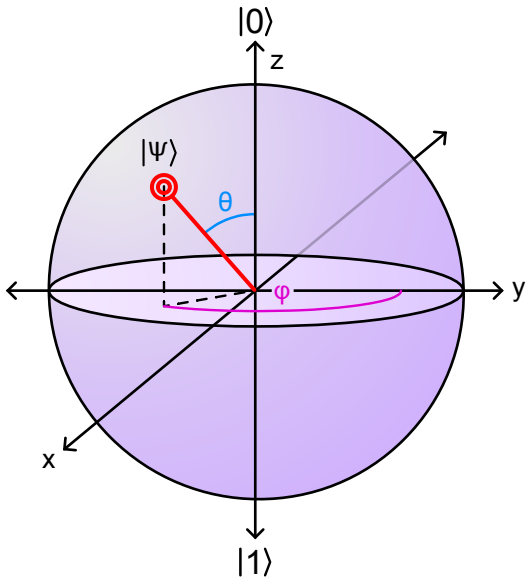

Figure 1.1: **The Bloch sphere.** The state of a qubit $|\psi\rangle$ visualised on a Bloch sphere. Singe qubits are always located on the surface of the sphere, described by the two angles θ and ϕ.

Moving the position of of a qubit $|\psi\rangle$ on the Bloch sphere to a different arbitrary location

can be done by multiplying the state of the qubit by an arbitrary *unitary matrix*.[1] The power of quantum systems comes from the unitary matrix, as the values within can be positive, negative, and complex.[2]

These unique characteristics enable quantum computers to efficiently solve BQP problems. A particularly strong example is based on the principle of classical and quantum random walks. Consider a random walk on a line. In the classical example, a coin flip allows for one step either forward or backward. Each subsequent coin flip results in a 50% chance of a forward or backward step from the previous position. So, over the course of five coin flips, the probability of taking five steps forward or backward is $\frac{1}{32}$. The probability of staying closer to the starting position is higher, taking on a Gaussian distribution at higher counts (see Fig. 1.2 (a)). Random walks on more complex structures are often used in classical algorithms.

In the quantum version of this example, instead of dealing with direct probabilities, we use the amplitudes mentioned previously. A balanced unitary coin is known as a Hadamard coin.

$$H = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{1.3}$$

Using a Hadamard coin vs. a traditional classical coin results in the quantum walk being distinctly different from a classical version, as shown in Fig. 1.2 (b) (for the interested reader, a detailed overview of how this Hadamard coin operates can be found at [28]).

Amplitudes, unlike probabilities, can take on negative values. Interference of these amplitudes changes the probability distribution. For instance, looking at Fig. 1.2 (b), the probability of being at position -1 after three steps is $3/8$ classically, but $5/8$ using the Hadarmard coin. After S steps, the classical distribution has a variance of $\sigma^2 = S$, and expectation values for distance from the origin are therefore $\sigma = \sqrt{S}$. The quantum random walk instead shows has a variance of $\sigma^2 \sim S^2$, with expectation values of $\sigma \sim S$. Here the quantum system explores the parameter space *quadratically* faster than its classical counterpart. Quantum computers exhibit polynomial, super-polynomial and sometimes exponential speedups of problems within the BQP complexity class, housed in disciplines that affect our daily lives such as encryption, chemistry, and material science.

[1] A matrix U is unitary if and only if $U^{-1} = U^*$.

[2] Classical systems use a stochastic matrix whose values are non-negative and real.

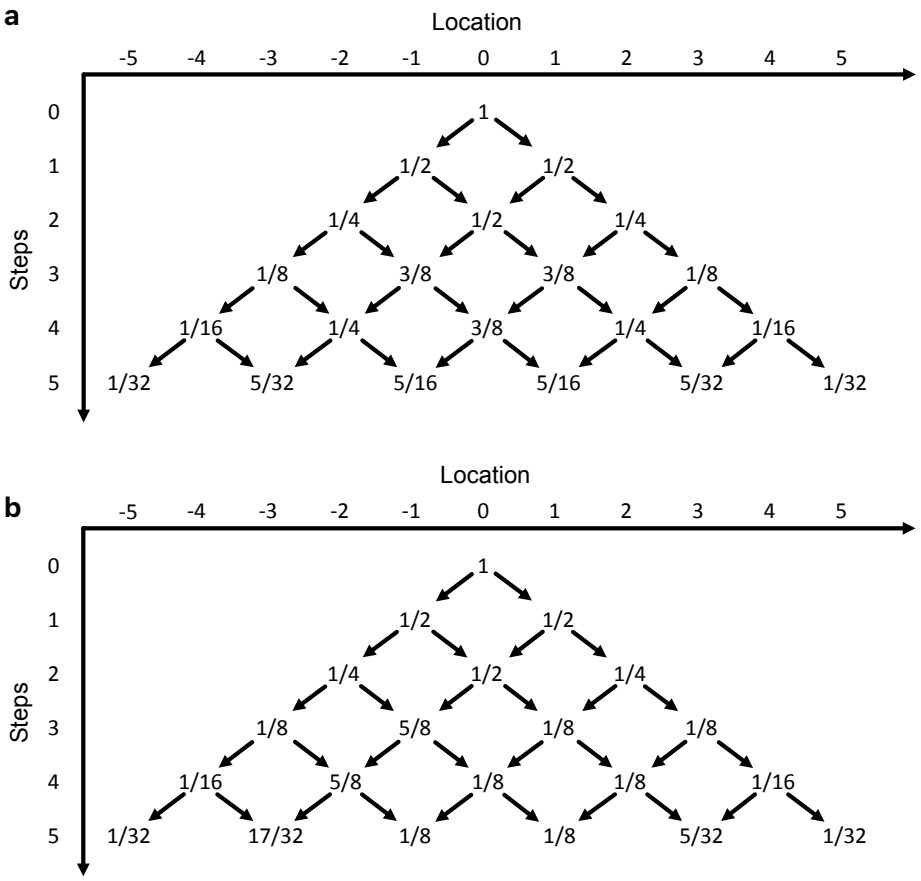

Figure 1.2: **Classical and quantum random walk. a**, A classical random walk based off of a coin flip. Each step has a 50% chance of going in a positive or negative direction relative to the starting location. Over many steps, the distribution is Gaussian. **b**, When using a Hadamard coin in the quantum random walk, amplitudes interfere in such a way to create a uniquely non-Gaussian-like distribution.

1.3 Burying the Lede

I've written phrases such as "serious challenge" and "monumental task" in reference to building a quantum computer, but haven't explained why. Unlike classical technologies, quantum systems are incredibly fragile, requiring extraordinarily quiet conditions in order to operate. Achieving a sufficiently quiet environment comes at the cost of an easily scalable system, and the efficient scale-up of qubit counts is the work of thousands of scientists worldwide. This is a ridiculous problem to try and summarize, instead I focus on the challenges principally surrounding the physical qubits: bottlenecks and error rates.

Bottlenecks

Every single qubit needs its own individual control, as the no-cloning theorem prohibits exact quantum states from being copied [29]. This is antithetical to their classical counterparts–the transistor–which is able to efficiently 'fan-out' by feeding output signals from one logic gate to the input for multiple gates (and vice versa). Instead of $\sim$ 1000 I/O lines for 10 billion transistors,[1] qubits demand at *minimum* 10 billion I/O lines if scaling by brute force alone.

The quietest environments are found at the lowest temperatures. Consequently, cryogenic refrigerators are commonly employed to cool down quantum systems. Squeezing billions of I/O lines into a cryogenic fridge requires novel and innovative approaches, as managing footprint and power dissipation emerge as primary challenges. Most research groups today operate less than 10 qubits, easily controlled and read using a number of transmission lines, but trying to use the same methods at much higher qubit counts generates a number of near-impossible tasks using a brute force approach. This I/O predicament can be categorized into two distinct challenges, each requiring separate solutions:

Control of spin qubits, a focus of this thesis, typically requires a combination of baseband gate pulses and high frequency microwave signals [30]. The inherent properties of cables capable of transmitting high-frequency signals render them unsuitable for large quantum systems comprising over one thousand qubits. The sheer number of cables introduce footprint, power dissipation, and noise challenges. Moreover, there exists an inherent speed limitation, as transmitting increasingly rapid pulses over extended distances places substantial demands on room temperature control equipment. Yet, this I/O bottleneck imposed by the physical size and cooling power of cryogenic fridges is only just starting to manifest for the largest systems out there. Investigation into efficient control schemes is a relatively recent endeavour compared to the decades devoted to advancing qubit performance. Presently, the best candidates for alleviating these challenges include introducing cryo-CMOS to locally generate baseband pulses, and employment of methods to efficiently generate microwave signals [7], eliminating the need for almost all the radio-frequency control lines. Chapter 5 explores cryo-CMOS control techniques.

Readout of large qubit counts presents similar challenges, but requires a separate set of solutions. Footprint concerns are arguably more pronounced for readout, given that the readout chain comprises bulky components such as circulators, amplifiers, and couplers. Like control, readout typically uses radio-frequency transmission lines, but in contrast these lines can be shared between a

[1] Based on current CPU architectures at the time of writing. Many of the contacts are for power, debugging, and redundancy.

large number of sensors. Frequency [9] and time division multiplexing increase the shareability, cutting down on both footprint and power dissipation from fewer active components. Dispersive sensing reduces the number of on-chip components [31], and parametric amplification [32] and cryo-analogue-to-digital converters [33] increase signal to noise ratio, allowing for more measurements in the same period. Beyond increased device sensitivity, this allows for even more time-division multiplexing. Chapter 4 examines dispersive readout of new architectures.

Implementation of these measures will not completely solve the bottleneck problem, but they are poised to form a substantial portion of evolving solutions. The diversity of quantum systems means these solutions are not universal, but they do hold relevance across condensed-matter qubit systems.

Performance

The operation of a physical qubit is one fraught with error. To enable universal quantum computation, physical qubits must be encoded into logical qubits endowed with error-correcting capabilities, ensuring resilience against errors. This critical threshold, known as the fault-tolerant threshold, mandates that physical qubits possess error rates of less than one percent [34]. Many qubits regularly exceed this threshold value, and reports of 99.9% are becoming ever more common [35–37]. Nevertheless, this is a far cry from classical computer DRAM error rates of 2.5×10^{-11} error/bit $\cdot$ h [38].[1] Even at error rates significantly below these current values, the number of physical qubits and operations to realize a single logical qubits still lies within the tens of thousands [39]. Suppressing these errors is a resource-intense exercise, using a combination of hardware (architecture) and software (dynamic pulsing) to reduce them as much as possible. Yet the sheer variety of errors and their ubiquity renders any qubit with less than 0.001% infidelity the stuff of dreams for most researchers.

Higher qubit counts come at the cost of qubit performance, and better qubits are harder to scale. These two challenges, almost diametrically opposed in their implications, must be addressed in tandem to enable utility-scale quantum computation. Achieving this goal is no trivial matter; it has taken the collective efforts of thousands of physicists nearly four decades to reach a stage

[1] The error calculation for classical hardware is slightly different to that of quantum hardware. Classical hardware measures error rates in terms of errors per bit hour. Quantum gate fidelities just measure error rate in terms of error per operation. This is due to the attempted 1:1 comparison between qubits (from quantum dots) and bits (from abstracted transistors) not being exact. At around 40GB per second read/write speeds, a 16 Gb stick DRAM can process close to 150 TB of data in an hour, leading to a single bit 'flipping' around 75,000 times per hour. So a single bit may undergo 3×10^{15} flips before experiencing a single error, compared to approximately 100 for the best qubits available today. I must emphasise these comparisons are not 1:1, bit it serves as an approximate comparison to the startling difference in error rates between classical and quantum hardware.

of significant commercial interest. Even so, a daunting amount of work is required to achieve fault-tolerant computation across a broad range of platforms. My research presented in this thesis constitutes a very small part of the path forward, while on a personal level it marks a significant milestone.

1.4 Thesis Aims and Scope

This thesis examines technologies and methods aimed at efficiently scaling up qubits. Although the devices presented here vary in architecture—utilizing gallium arsenide and silicon, respectively—the readout and control mechanisms are compatible with both. Notably, these approaches can be seamlessly integrated into CMOS fabrication methods, a crucial aspect as the quantum computing sector shifts towards large-scale industrial fabrication. The studies within this work provide compelling evidence that these technologies will not only be beneficial but perhaps essential for realizing large-scale qubit arrays. Together, they constitute a suite of technologies poised for seamless integration into today's rudimentary devices.

The scope of this thesis is organized as follows:

Chapter 2

This chapter explores the fundamental physics of mesoscopic and microscopic systems that interact with qubits. Taking a bottom-up approach, the physics of two- and one-dimensional systems are outlined, with a focus on GaAs architectures but generalizable to other approaches utilizing a two-dimensional electron gas. In particular, I explore dynamics of two-dimensional and one-dimensional systems within a magnetic field. Further dimensional restriction forms quantum dots, which are presented within the framework of a constant interaction model. Finally, I explore methods for fast readout of emergent quantum properties in these systems, essential to the operation of utility-scale quantum computers.

Chapter 3

An electron in a magnetic field exhibits behavior compatible for encoding of quantum information to form a qubit. Chapter 3 explores the fundamentals of a qubit, before detailing a few encoding methods that form the foundation of several university and research organisation efforts for realizing a general-purpose quantum computer. Focusing on spin encoding, the dynamics and operation of a single spin qubit are presented. The addition of a second qubit complicates the

picture, necessitating exploration of two-qubit interactions, operation, and more advanced gate sets to characterize the performance of single- and two-qubit systems. Adding a further ten billion qubits again creates more problems, which I attempt to summarize.

Chapter 4

Chapter 4 explores the detection of the Aharonov-Bohm phase with gate reflectometry in a GaAs substrate. Phase detection on fast timescales is demonstrated, providing a path forward for a measurement-only approach to topological quantum computation. Two devices with differing design are measured, and evidence of phase detection is present in both. Radio-frequency probing of the phase yields similar Aharonov-Bohm period and phase compared to a traditional direct-current approach. This new detection technique is only sensitive within a narrow window set by the coupling of the detection probe (a quantum point contact or quantum dot) to the ring structure.

Chapter 5

Chapter 5 presents data showing coherent control of silicon spin qubits using a proximal cryo-CMOS module at millikelvin temperatures. Single and two qubit gates are realised, and compared against their room temperature controlled counterparts. Little effect on coherence and qubit fidelity is found. Exploiting a DC Stark shift allows for a global control method using cryo-CMOS, eliminating the need for high-power microwave lines. The qubits are also used as a noise probe, to examine the effects of various cryo-CMOS chip parameters, finding thermal contributions to be largest noise source.

Chapter 6

This chapter places the experiments in this thesis into the broader challenge of qubit system scale-up. Potential future implementations and improvements are highlighted, and a future outlook on the wider field of quantum computing is discussed.

Appendix A

Appendix A presents additional data supporting the findings in Chapter 4.

Appendix B

Appendix B provides further information on the methods used in Chapter 5. Many of these techniques work behind the scenes to improve qubit performance.

Appendix C

Appendix C presents a time-division multiplexing experiment, aiming to reduce the per-qubit readout resources needed for highly scaled systems.

Appendix D

Appendix D details nanofabrication recipes for GaAs devices.

Appendix E

Appendix E explores in more detail the physics, fabrication, and performance of ohmic contacts in GaAs devices.

Appendix F

Appendix F contains additional information on cryogenic operation. The physics of a dilution refrigerator, specifics on dc and high frequency line setup, cooling power, and thermalization is discussed.

2

Foundations of Quantum Systems

Ask any experimental quantum researcher, and they will passionately argue why their chosen architecture surpasses all others. I intend on doing the same, as *spin qubits* emerge as the prime candidate for large-scale quantum computation which will become clear in the next two chapters. In brief, spin qubits are extremely small, fast, and long lived, allowing for many qubit operations before errors rear their head. This chapter explores the physics behind the qubits, the very foundation (i.e. bulk substrate) upon which they are made. Specifically, I focus on two implementations: GaAs and Si quantum dot systems. Both platforms are adept at forming two-dimensional, one-dimensional, and zero-dimensional (quantum dot) states, wherein we uncover novel physics that govern these quantum systems.

Silicon and gallium arsenide semiconductors are intricately linked, as both possess properties conducive to the manufacture of transistors and qubits. While certain characteristics of silicon are advantageous for the operation of billions of qubits—partly due to 50 years of semiconductor industry research—both systems are excellent for researching scalable control and readout techniques. Beyond the DiVincenzo criteria [40], spin qubits require systems with (1) high energy splitting and (2) a large Fermi wavelength λ_F. These practical considerations ensure quantum information is accessible from a noise and fabrication capability standpoint. Operating these quantum systems, however, demands extremely low temperatures.

When the thermal energy of an electron, $k_B T$, is significantly smaller than energy splitting[2], it opens avenues for exploring an electron's fragile quantum properties. At 0 K, the highest en-

[2] This is purposefully vague as energy splitting can come in many forms, for example quantized occupation, Zeeman splitting, valley and orbital splitting, and many more.

ergy electron state is defined as the Fermi energy, E_F. In metals, this Fermi energy resides within the conduction band. However, in semiconductors, it is positioned between the conduction and valence bands. This poses an advantage for quantum systems, as the electrons can be precisely moved and trapped using electric fields, a much harder prospect in a conductive material. Additionally, building nano-scale structures for semiconductor systems is easier too, as these structures don't have to be as small compared to metallic systems. This is due to a difference in the Fermi wavelength λ_F, a characteristic describing the 'size' of an electron in a medium.

The Fermi wavelength, λ_F, is given by:

$$\lambda_F = \frac{h}{\sqrt{2m^* E_F}} \tag{2.1}$$

where m^* is the effective mass of the electron. Effective mass is used to give the correct numerical value when applying the equations of electrodynamics to electrons (or charge carriers in general) in a solid. The effective mass changes due to electron interactions with the periodic potential of the lattice structure of the solid. GaAs has an effective electron mass of $m^* = 0.066\, m_e$, whereas in Si it is approximately $m^* = 0.19\, m_e$ where m_e is the free electron rest mass. This small effective mass leads to a large Fermi wavelength λ_F at > 10 nm vs. ~ 0.5 nm or smaller in most metals. This length is within fabrication capabilities to lithographically define structures that form qubits, the specifics of which are detailed in Chapter 3.

2.1 Two-Dimensional Systems

Confining electrons to two dimensions unlocks a new realm of physics to explore. Understanding the environment of a two-dimensional electron gas (2DEG) is crucial as it forms the foundation of many spin qubit systems. Qubits are only as good as the potential landscape they inhabit, so building the cleanest interface possible is the best start to making well-functioning quantum systems. The following section explores the construction of a two-dimensional electron gas, the quantum dynamics that happen at different length scales and emergent phenomena based on the presence of a magnetic field. Sections 2.1 and 2.2 follow the physics of transport in GaAs systems, before we rejoin with silicon-based architectures to understand quantum dots.

2.1.1 The Two Dimensional Electron Gas

There are many ways of creating a two-dimensional landscape. A common theme among them is the joining of dissimilar materials, where the physics at the interface allows for the formation

of a 2DEG. In pure silicon architectures, this is right at the surface: at the junction between Si and SiO_2. In gallium arsenide systems, the picture is more complex, with the 2DEG forming at the interface between gallium-arsenide (GaAs) and aluminium-gallium-arsenide (AlGaAs). The physics and construction of GaAs/AlGaAs 2DEGs is explored further in this section.

At the discontinuity, band bending occurs as a result of unequal Fermi energies, leading to the formation of a triangular potential well (see Fig. 2.1). The width of the well is on the order of the Fermi wavelength, confining free electrons to two dimensions only. Importantly, the lattice constants between GaAs and AlGaAs remain nearly identical, facilitating a smooth transition and minimizing boundary scattering. This characteristic contributes to significantly higher electron mobility compared to similar MOSFET devices, an important aspect for quantum systems as it leads to reduced scattering and noise and lower power dissipation [41].

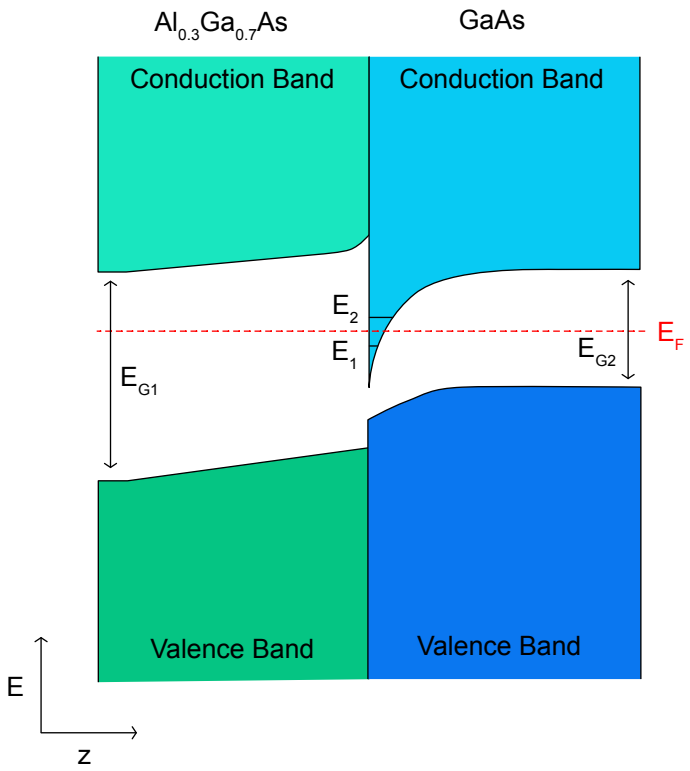

Figure 2.1: **2DEG heterojuction band bending**. At the junction between AlGaAs and GaAs, the bands bend to preserve the continuous Fermi energy. The straddling junction here creates a potential well. At low temperatures the sub-bands E_1 and E_2 lie close to the Fermi energy E_F, with E_1 able to be occupied at ground state energy levels.

The ratio of aluminium to gallium ($Al_{1-x}Ga_xAs$) is determined by the limits of direct bandgap

behaviour, constraining x between 0 and 0.44. While the bandgap of GaAs remains fixed at $E_{\text{GaAs}} = 1.4$ eV, the bandgap of AlGaAs varies with x, following the equation $E_{\text{AlGaAs}} = 1.424 + 1.225x$ eV. At room temperature, a typical value for E_{AlGaAs} is 1.8 eV, spanning the smaller E_{GaAs} gap [42].

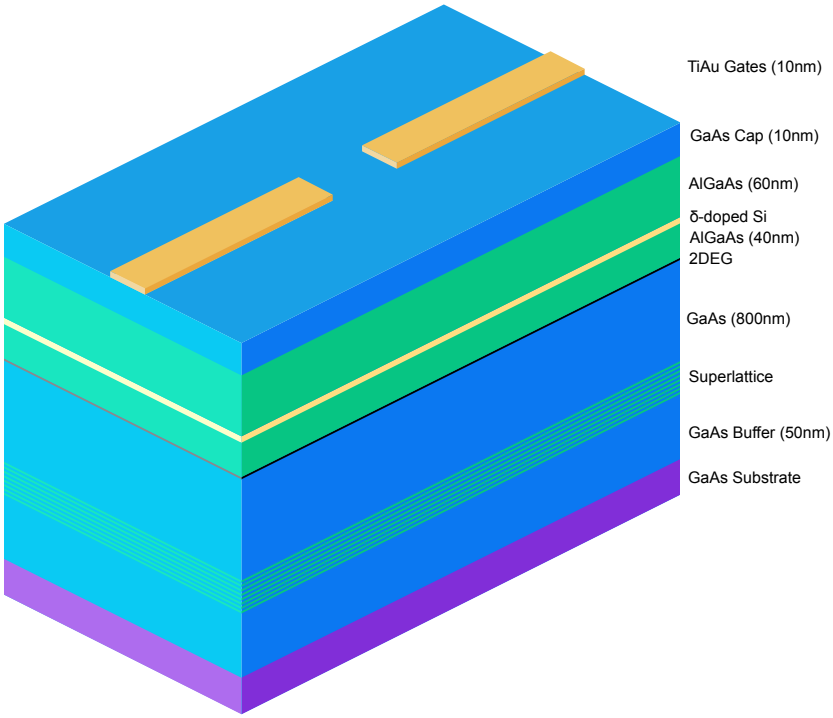

Figure 2.2: **GaAs heterostructure material stack.** A GaAs/AlGaAs heterostructure, on which many of the experiments of this thesis are based. The 2DEG junction, indicated by the black line, resides about 91 nm below the surface of the chip. The superlattice contains 30 bands.

Fabricating heterostructures involves a complex, multi-step process that demands specialized techniques. It begins with a GaAs wafer serving as the foundational substrate, onto which a GaAs buffer layer is grown to facilitate the subsequent layers' growth[1]. Following this, a superlattice consisting of alternating layers of GaAs and $Al_{0.3}Ga_{0.7}As$ is grown. This superlattice serves to trap impurities and defects originating from the stock wafer before they can affect the heterostructure junction. Another GaAs buffer is grown to suppress any secondary effects of the superlattice. Subsequently, $Al_{0.3}Ga_{0.7}As$ is deposited atop this layer, forming the heterostructure junction.

A silicon δ-doping layer 40 nm above the junction populates the heterostructure. The dopants are ionized, and electrons from this doped layer become trapped within the AlGaAs/GaAs junction. At low temperatures, typically a single subband within the interface is populated. Modu-

[1]Molecular-beam epitaxy (MBE) is employed for precise monolayer deposition of materials.

lation doping enables the separation of the doping layer from the junction, a technique crucial for controlling the Fermi level within the substrate and minimizing scattering due to Si impurities. Finally, a GaAs cap layer is added for oxidation protection.[1] Local fabrication, involving processes such as etching and deposition of specific metals and oxides, enables the realization of one-dimensional systems and quantum dots, topics discussed in the following sections.

2.1.2 Transport Properties

An electron in a potential plane is guaranteed to encounter impurities and other scattering phenomena that limits the distance over which it preserves quantum information. By knowing what these distances are, we can create structures within that bound to preserve the electron's quantum properties. Generally there are two kinds of scattering: elastic and inelastic. Elastic scattering preserves an electron's momentum, and occurs when interacting with an object of much higher mass. Inelastic scattering, on the other hand, does not preserve momentum, and is more likely to occur due to an interaction with an object of similar mass. In this model elastic scattering is more common than inelastic scattering, meaning they constitute two different length scales, quantum ballistic and diffusive (l_e and l_i respectively). The distance travelled before an interaction is dependent on the density of scattering sites within a medium, such that along the same path $l_e < l_i$. Ballistic and diffusive transport regimes are therefore defined as:

$$\text{Quantum Ballistic: } \lambda_F \sim L \ll l_e < l_i \tag{2.2}$$

$$\text{Quantum Diffusive: } l_e \ll L < l_i \tag{2.3}$$

An electron scattering off impurities, defects, and edges is likely to undergo elastic scattering with almost no energy exchange, preserving its momentum. Quantum dots and quantum point contacts are formed in the quantum ballistic transport window, as discrete energy modes occur in the direction of confinement.

As path length L increases, the probability of an inelastic scattering event increases with the number of total interactions. Inelastic scattering is an energy-exchanging interaction, and is much more likely to occur due to time-dependent mechanisms such as phonon interactions, as they have energy and mass similar to that of an electron. The inelastic scattering length l_i is closely linked to the thermal temperature of the sample, as more phonons are present at higher temperatures [43].

[1] Growth of AlGaAs/GaAs heterostructures is done off site by a research group headed by Michael Manfra, who's fabrication abilities are much more specialised towards this particular process. Therefore heterostructures with varying depths and degrees of mobility can be grown with extreme precision. All other fabrication is done locally.

In this window, phase information is preserved, leading to the emergence of phase-coherent effects such as the Aharonov-Bohm effect (Section 2.2.2) and weak localization.

2.2 One-Dimensional Systems

Unlike the confinement in a 2DEG, the one-dimensional transport discussed in this thesis stems from electrostatic or magnetic constraints, affording a high level of control over the energy modes within the channel. A system qualifies as quasi-one-dimensional when the channel width l_x approximates the Fermi wavelength λ_F. Within such systems, multiple energy modes may emerge within a single channel, originating from transverse momenta k_x akin to bound states. A current through a one-dimensional channel becomes *quantized*, such that:

$$I = \frac{2e^2}{h} V_{SD} \tag{2.4}$$

where V_{SD} is the source-drain voltage difference across the channel. Usually, we redefine transport through a one-dimensional channel in terms of quantized conductance:

$$G = \frac{NI}{V_{SD}} = N\frac{2e^2}{h} \tag{2.5}$$

where N is the number of filled modes.

For a more realistic approach of quantized conductance, two modifications need to be made. At first, we assumed each electron that entered the channel transmitted through. This transmission is in fact probabilistic. Electron wavefunctions can sometimes transmit only partially through the channel with a full transmission probability of T_n for each mode n, where $T_n \leq 1$. The conductance can be written as the Landauer formula:

$$G = \frac{2e^2}{h} \sum_{n=1}^{N} T_n \tag{2.6}$$

The second consideration takes into account the thermal smearing effects due to the temperature dependence of the Fermi-Dirac distribution:

$$f(E - E_F) = \left[1 + \exp\left(\frac{E - E_F}{k_B T}\right)\right] \tag{2.7}$$

Seen in Fig. 2.3, the Fermi-Dirac distribution, as its name suggests, creates distribution of filled

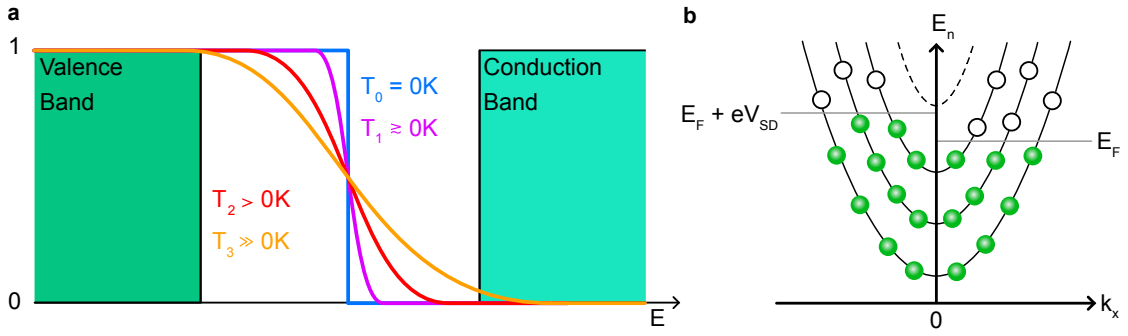

Figure 2.3: **Thermal broadening and dispersion relation. a**, Fermi-Dirac distribution as a function of temperature. At higher temperatures the distribution spreads out, penetrating the conduction band and allowing for free electrons to travel within the heterostructure at locations not within the 2DEG and not restricted to two dimensions. **b**, The dispersion relation for electrons travelling through a one-dimensional channel. Some empty states (white) are filled on the left due to an applied bias.

states. The thermal energy $k_B T$ of the system must be minimised to avoid such a distribution as to blur out some of the more fragile quantum effects. Conductance can be rewritten as:

$$G(E_F, T) = \frac{2e^2}{h} \sum_{n=1}^{\infty} f(E_n - E_F) \tag{2.8}$$

For heterostructure systems, thermal smearing begins to fully wash out quantized steps near 4 K.

These 1D channels are realised in heterostructure systems via a number of different means. Here I will cover three: Hall bars, Aharonov-Bohm rings, and quantum point contacts. Each is one-dimensional over a different path length L, revealing new physics along the way.

2.2.1 The Quantum Hall Effect

Although not directly measured in this thesis, understanding the quantum Hall effect is paramount for understanding the dynamics outlined in Chapter 4. Arising alongside phenomena like the Aharonov-Bohm effect and Shubnikov-de Haas oscillations, the quantum Hall effect originates from similar quasi-one-dimensional transport dynamics within mesoscopic systems. These phenomena are intricately interconnected, making it challenging to analyze one in isolation from the others. In experimental settings, it's common for multiple such phenomena to coexist simultaneously. In this section, I look at both the classical and quantum facets of the Hall effect, before

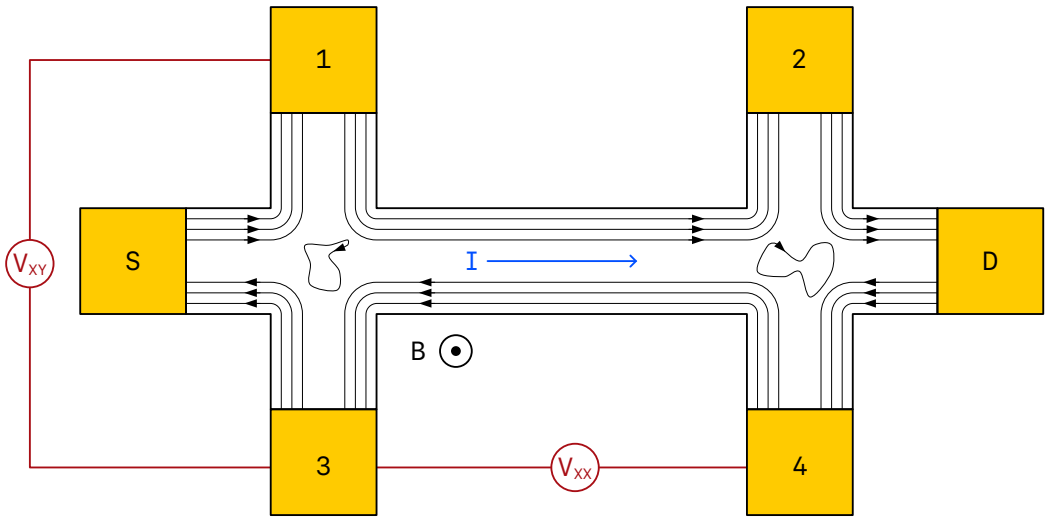

Figure 2.4: **Current flow in a Hall bar**. Schematic of a 2DEG-based Hall bar, illustrating the edge states that form under high magnetic field. Ohmic contacts are yellow and the current flow through the device is indicated. Longitudinal and transverse voltage V_{xx} and V_{xy} are measured as shown, between ohmics $3 \rightarrow 4$ and $1 \rightarrow 3$ respectively. By knowing the length and width of the 2DEG channels, fundamental 2DEG quantities can be derived from measurements.

introducing the theory behind Shubnikov-de Haas oscillations. This is only a brief overview, covering the basics and relevant bits to my research, and for the interested reader a more comprehensive review can be found at refs. [44, 45].

Classical Hall effect

In the presence of a perpendicular magnetic field B, electrons within a 2DEG undergo cyclotron orbits driven by the Lorentz force. The radius of these orbits is contingent upon the magnetic field strength. Electrons at the edge of the 2DEG fail to complete full orbits, instead traversing along the sides, inducing a charge differential and an electric field E across the sample proportional to B. This voltage drop, perpendicular to the current flow, constitutes the Hall voltage [46].

Investigation of the Hall effect in 2DEG materials is often employed using a Hall bar (refer to Fig. 2.4). Consisting of between five and eight ohmic contacts, a Hall bar enables the measurement of longitudinal (xx) current, as well as longitudinal and transverse (xy) voltages. Precise determination of the Hall bar's dimensions allows for the extraction of fundamental characteristics of the 2DEG, including mobility, density, and Fermi wavelength, from these measurements.

The radius of the circular electron paths is:

$$R_c = \frac{m^* v_F}{eB} \tag{2.9}$$

where v_F is the Fermi velocity.

Quantization

The quantization of the classical Hall effect occurs when $R_c \ll l_e$. One-dimensional electron edge transport undergoes a transformation into discrete energy bands, known as Landau levels, which exhibit high degeneracy. These discrete energy levels rise at the edges of a Hall bar [45], intersecting the Fermi energy level E_F. At these intersections, electrons populate newly available states, leading to significant changes in the Hall resistance as a function of magnetic field. This quantization of energy states yields powerful consequences, including its role in defining fundamental constants such as the Ohm:

$$\frac{h}{e^2} = \frac{\mu_0 c}{2\alpha} = 25812.80767\,\Omega \tag{2.10}$$

where μ_0 is the permeability of free space, c is the speed of light and α is the fine structure constant [47, 48].

Skipping the Hamiltonian formalism, Hall conductance becomes:

$$\sigma_H = \frac{I}{V_R - V_L} = \frac{2ne^2}{h}, n = 1, 2, 3, ... \tag{2.11}$$

where n is the occupied Landau level number. The Hall conductivity can be rewritten rewritten as:

$$\sigma_H = \nu \frac{e^2}{h} \tag{2.12}$$

where ν is the number of electrons per quantum magnetic flux, known as the filling factor [49]. Filling factor ν takes on integer values in the integer quantum Hall effect regime (as the name suggests), and can further occupy precise fractional values as a fractional quantum Hall regime. Fractional states are beyond the scope of this thesis, and I point the interested reader to the following references for more detail on the subject: [50, 51].

Shubnikov-de Haas effect

Before the full quantization of conductance at high magnetic fields and the subsequent discovery of the quantum Hall effect, scientists had already noted peculiar oscillations in channel conductance

with varying magnetic fields [52]. These oscillations, termed Shubnikov-de Haas (SdH) oscillations, play a crucial role in understanding the unusual conductance behaviors exhibited by mesoscopic materials. As depicted in Fig. 2.5, when measured in a Hall bar the longitudinal current experiences a gradual decline as the magnetic field B intensifies. Around the threshold of approximately 250 mT, an intriguing phenomenon unfolds: the conductance assumes a sinusoidal modulation, with its frequency exhibiting periodicity in $1/B$. This distinctive behavior arises when the separation between Landau levels exceeds the level broadening, a condition represented by $\omega_c\tau \approx 1$, where τ symbolizes the scattering time and $\omega_c = l_e/\tau R_c$. The circular electron paths are spaced equally in energy, acting like a simple harmonic oscillator:

$$E_n = \hbar\omega_c \left(n + \frac{1}{2}\right) \pm \frac{1}{2} g^* \mu_B B \tag{2.13}$$

where the Laundau level is defined by n, μ_B is the Bohr magneton and g^* is the effective Landé g-factor. From here, a relation of magneto-resistance to the SdH effect can be found as [45]:

$$\frac{1}{B} = \frac{n_s n_v}{n_D} \frac{e}{h} \left(n + \frac{1}{2}\right) \tag{2.14}$$

where n_D is the 2DEG density. QHE occurs at higher fields, where magneto-resistance drops to zero between peaks.

2.2.2 The Aharonov-Bohm Effect

By confining one-dimensional transport to a phase-coherent regime, new conductance behaviors emerge. Among the phenomena encountered is the Aharonov-Bohm (AB) effect, initially theorized in 1959 [53] and experimentally confirmed in the early 1985 [54]. In a restricted ring geometry, the magnetic flux Φ becomes well-defined, leading to periodic conductance fluctuations as a function of the perpendicular magnetic field B. The observation of these fluctuations serves as compelling evidence that both magnetic and electric potentials, denoted by $\mathbf{A}$ and φ respectively, exert tangible physical effects. This notion is supported mathematically, as certain potentials cannot be algebraically eliminated from certain Hamiltonian equations.

The Aharonov-Bohm effect can be conceptualized by envisioning the splitting of electron trajectories around an ideal infinite solenoid, like in Fig. 2.6. The Hamiltonian for this system is:

$$H = \frac{1}{2m} \left(-ih\nabla - q\mathbf{A}\right)^2 \tag{2.15}$$

with solutions

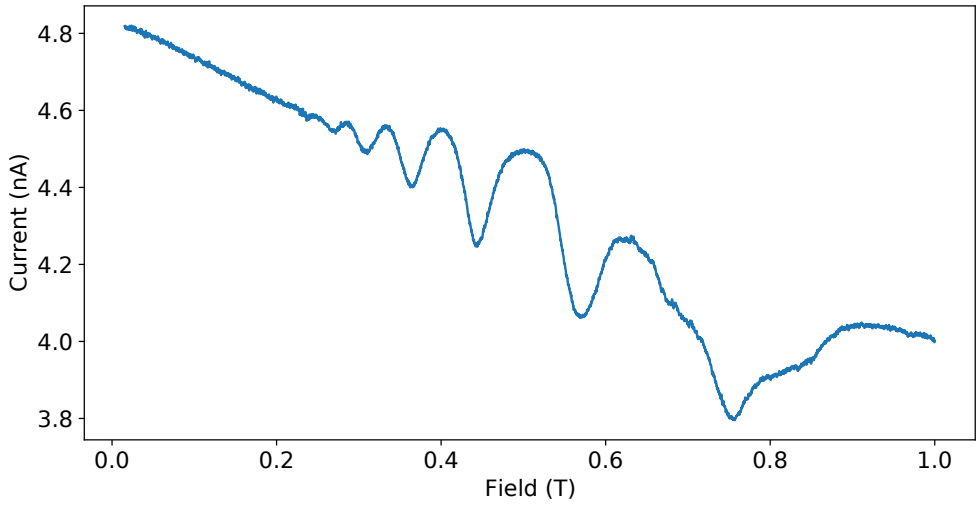

Figure 2.5: **Shubnikov-de Haas oscillations in a GaAs/AlGaAs Hall bar**. Variations in the longitudinal current as a function of magnetic field. At approximately 250 mT, Landau separation matches energy broadening, resulting in SdH oscillations that grow in amplitude as a function of B. At higher magnetic fields, the SdH oscillations distort as we approach separation necessary for QHE phenomena to form.

$$\psi = \psi_0 e^{ig(\mathbf{r})} \tag{2.16}$$

where

$$g(\mathbf{r}) = \frac{q}{\hbar} \int \mathbf{A} \cdot d\mathbf{r} \tag{2.17}$$

and ψ_0 is a solution when $\mathbf{A} = 0$.

In regions $\mathbf{r} > s$ where s is the radius of the solenoid, magnetic potential $\mathbf{A}$ is given by

$$\mathbf{A} = \frac{\Phi}{2\pi r}\hat{\phi} \tag{2.18}$$

where $\hat{\phi}$ is counterclockwise and Φ is the enclosed magnetic flux. The two Feynman paths around the ring experience phase shifts, due to their directionality in comparison with $\mathbf{A}$. The phase difference θ_d between the two paths is

$$\theta_d = \frac{q}{\hbar} \oint \mathbf{A} \cdot d\mathbf{r} \tag{2.19}$$

and integration over this closed path gives

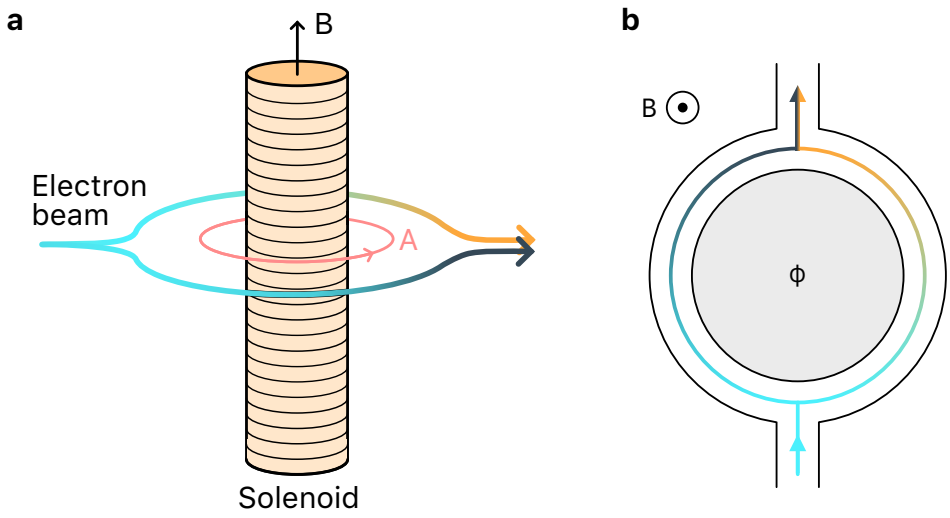

Figure 2.6: **Schematic of the AB effect geometry**. **a**, Schematic of an ideal experiment to demonstrate the AB effect. The two paths of coherent electrons pick up different phases due to the presence of the magnetic potential **A** outside the solenoid. Magnetic field **B** is completely contained within the solenoid. **b**, Ring geometry to observe the AB effect. Realistically, the flux Φ penetrates the inner ring as well as the ring paths.

$$\theta_d = \frac{q\Phi}{\hbar} \tag{2.20}$$

The AB effect can be measured in 2DEG systems with simple ring structures, akin to the one detailed in Chapter 4. In such experiments, the magnetic field B permeates both the arms of the ring and its internal flux area. Although deviations from Equation 2.20 are anticipated if the enclosed flux Φ is strictly defined as the inner ring area alone, these deviations are minimal and unlikely to cause any significant concern for experimentalists.

Experimental observation of the AB effect is possible by gradually increasing the perpendicular magnetic field, thereby altering the flux passing through the ring. This results in observable oscillations in conductance due to the modulation in phase interference, as depicted in Fig. 2.7. Each individual oscillation corresponds to a flux variation of one flux quantum: $\Phi_0 = h/e$. Consequently, the period of the AB oscillations, denoted by ΔB, is determined by this flux change:

$$\Delta B = \frac{\Phi_0}{S} = \frac{h}{e}\frac{1}{\pi r^2} \tag{2.21}$$

where r is the ring radius. Typically, ΔB is known through measurements and r is calculated.

The 2DEG introduces further complications to this idealised picture due to considerations of feature size and additional physics. AB rings are subject to fundamental size constraints, with path

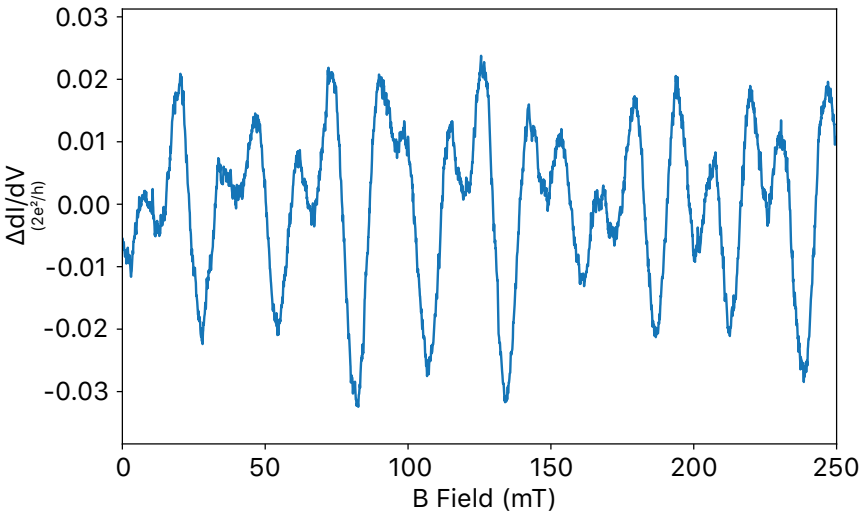

Figure 2.7: **AB oscillations as a function of magnetic field in a GaAs 2DEG.** Constructive and destructive interference leads to an oscillating signal as the perpendicular magnetic field is ramped. Altshuler-Aronov-Spivak oscillations are also present.

lengths smaller than the Fermi wavelength risking additional noise from self-interference, while longer path lengths than the phase coherence length result in the loss of all phase information before recombination. Moreover, the ring width plays a crucial role; at higher magnetic field values, if cyclotron diameters shrink to sizes smaller than the ring width ($2R_c < W$), the AB effect can be suppressed due to one-dimensional Hall-effect transport along the inner and outer edges of the ring [55, 56]. Additionally, coherent backscattering of electrons can lead to the emergence of higher harmonics. The first harmonic, termed Altshuler-Aronov-Spivak (AAS) oscillations, is frequently observed in 2DEG rings. In this phenomenon, the electron path accumulates twice the phase difference, resulting in a doubling of the oscillation frequency [57, 58].

2.2.3 The Quantum Point Contact

Finally, confining the path length L of a one-dimensional channel within the quantum ballistic regime allows one to engineer a quantum point contact (QPC). This device holds paramount importance, often serving as a tool for reading out quantum states. Unlike Hall bars and Aharonov-Bohm rings, QPCs are almost always realised electrostatically. This allows for much finer tuning of the 1D channels for maximum sensitivity. Once again, the conduction through the channel is quantized, and when positioned in close proximity to a system under investigation, the QPC operates as an exceedingly sensitive charge sensor, capable of detecting even minute changes in the system.

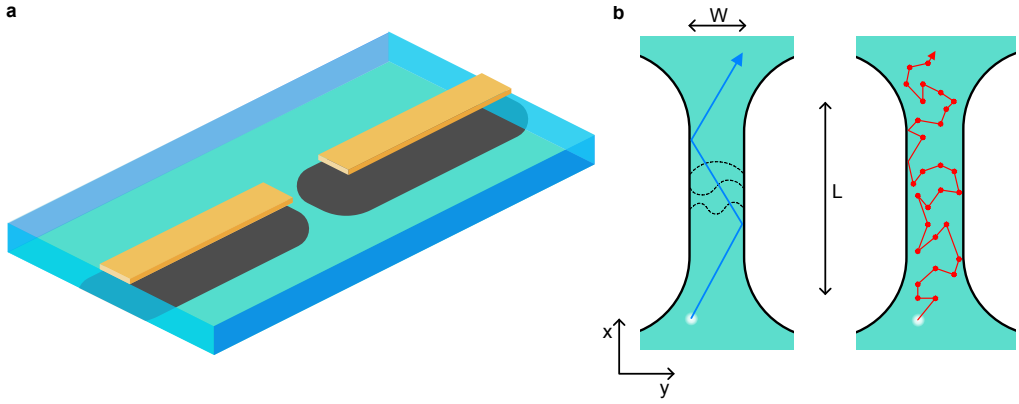

Figure 2.8: **QPC design and transport. a,** Effect of negatively biased gates on the surface of a heterostructure on the 2DEG underneath. Dark grey regions indicate areas where electrons are depleted. With the right tuning, a one dimensional channel between the two gates forms. **b,** An example of ballistic transport through the channel. Electron paths (blue) scatter elastically off the wall of the system, preserving momentum and phase. The first three allowable electron energy modes are shown as wave-functions with wavelength $\lambda = 2W$, $\lambda = W$ and $\lambda = 2W/3$ respectively. On the right shows diffusive transport through the system. An electron inelastically scatters off of many impurities, randomizing the momentum and phase.

Back Action

The delicate nature of quantum systems renders QPCs, like many other quantum systems, highly susceptible to environmental fluctuations. Moreover, they possess the capability to induce changes in the environment that may adversely affect other quantum systems. When current flows through a QPC, energy is dissipated in the form of phonons, photons, or electron-electron scattering. Each of these mechanisms introduces noise into the quantum system. However, the magnitude of this noise, as well as the dominant mechanism(s), hinges on various factors including the temperature

of the system, the energy disparity between the reservoirs, and the proximity of the QPC to the quantum dots. In this thesis, the average temperatures and separation distances are approximately 20 mK and 200 nm, respectively. At these scales, phonon excitation of a quantum dot emerges as the predominant form of back-action [59]. Notably, acoustic phonons generated by QPC back-action exhibit wavelengths akin to the separation distance of the quantum dots [60, 61].

As depicted in Fig. 2.9, when a phonon interacts with an electron within a quantum dot, the phonon can excite the electron to an energy level beyond that of the confining potential. Consequently, the electron vacates the quantum dot, destroying any quantum information it may posess in the process. Mitigating this perturbation comes with certain costs. Analogous to Heisenberg's Uncertainty Principle, placing a QPC in closer proximity for more sensitive measurements may exacerbate the extent of back-action experienced by quantum dots. Further discussion of readout techniques is found in Section 2.4.

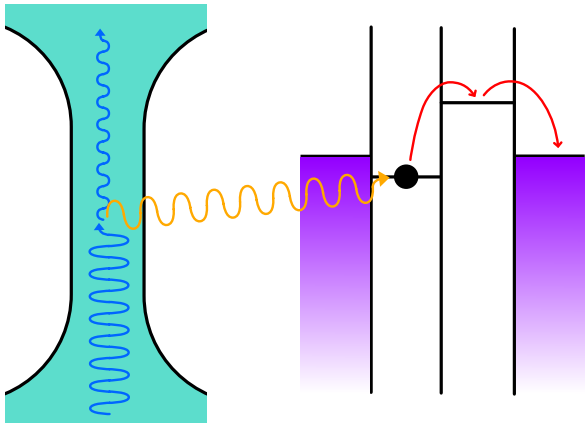

Figure 2.9: **QPC back-action.** An electron travelling through a QPC experiences back-action fluctuations, generating a phonon in the process. Travelling in the correct direction, the phonon interacts with a ground state quantum dot, exciting it into a state where it can leave the system entirely.

2.3 Quantum Dots

Throughout my PhD journey, every significant experiment I performed has involved *quantum dots*. These are minute areas where electrons can be trapped in all three dimensions, essentially creating zero-dimensional systems. Quantum dots, regardless of heterostructure or substrate, stand as

the cornerstone of quantum computers in condensed matter systems. Their ubiquity lies in their ease of construction. In 2DEG structures, for instance, creating a small island of electrons requires little more than placing the gates to create a confinement-like structure. In some silicon architectures, the process is even simpler as quantum dots form beneath the gates themselves. Within these dots, electrons occupy a discrete energy spectrum of available states [62], mimicking the behavior of "artificial" atoms with orbital modes. By minimizing the electron count within each quantum dot to countable values, we establish the physical foundation for charge- and spin-based qubits.

The positioning, dimensions, and interaction of quantum dots with surrounding systems are all dictated by the tuning and placement of gate electrodes. Understanding the behavior of quantum dots under specific conditions, and how to tune to those conditions, is key to qubit creation. The type, size, and layout of these dots yield considerable influence over the ultimate performance of the qubits. This section covers the basic physics of single- and double-quantum dots, the foundation for the rest of this thesis.

2.3.1 Single Quantum Dots

Single quantum dots are some of the simplest structures that may be found in a quantum computer. Modelling the dynamics of a single quantum dot can be complex, however some of this complexity can be reduced by assuming that the Coulomb interactions between the dot and its environment is parameterized by constant capacitances. Known as the constant interaction model, this method is suitable for understanding the basics of how a quantum dot works.

The total energy is described as a function of charge, voltages on the gates, and bias on the reservoirs. Here,

$$U(N) = \frac{[-e(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{2C_\Sigma} + \sum_{n=1}^{N} E_n(B) \tag{2.22}$$

where N is the total number of electrons, N_0 is the background charge,[1] C_S, C_D, and C_G, are the capacitance and voltage values of the source, drain and gate electrode, C_Σ is the total capacitance, and E_n is the sum of energies of the electrons at levels n, dependent on the magnetic field. We assume that varying only a single gate is required to change electron occupancy in the dot. Adding a single electron requires energy:

$$E_{add}(N) = \frac{e^2}{2C_\Sigma} + \Delta E \tag{2.23}$$

[1] N_0 is defined as $N_0^2 = E_F/E_C$ where E_C is the charging energy.

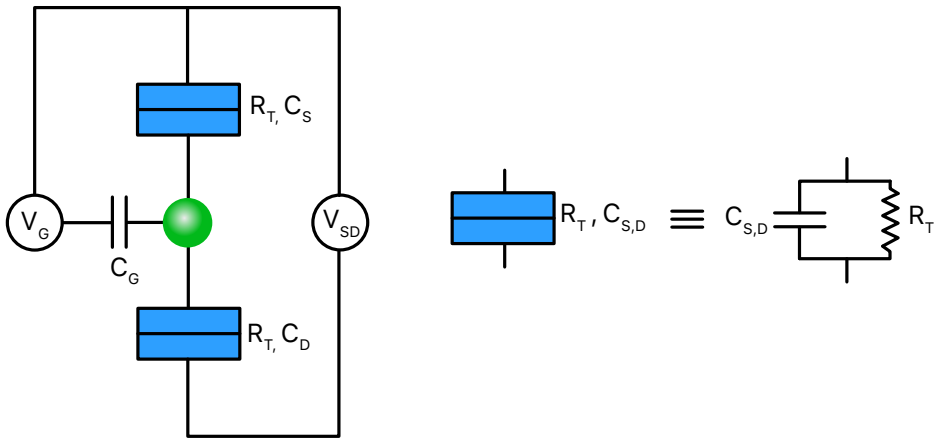

Figure 2.10: **Circuit model of a quantum dot.** Tunnel junctions connect the dot to the source (S) and drain (D) reservoirs, via a parallel capacitance and resistance. The tunnel resistance R_T and geometric capacitance to the source and drain $C_{S,D}$ are functions of the voltage V_{SD} as well as the physical layout of the system. The dot is capacitively coupled to the defining gates (we assume the primary gate tuning the dot levels has a voltage V_G) with a capacitance of C_G.

where ΔE is the level spacing between electrons. Charging energy E_C is defined as $e^2/2C_\Sigma$. This is similar to the energy of a capacitor $E = Q^2/2C$, meaning a simplistic quantum dot can be modelled as a pool of charge in a classical electrical circuit, like in Fig. 2.10. The electrochemical potential for a single quantum dot is defined as:

$$\mu(N) = U(N) - U(N-1) \tag{2.24}$$

leading to the addition of an additional electron requiring energy:

$$E_{add}(N) = U(N+1) - U(N). \tag{2.25}$$

This energy cost of adding an extra electron is due to Coulomb repulsion of electrons in the dot. At low temperatures the addition of an electron is suppressed, as the electrostatic energy of an electron $E_{add}(N)$ is much greater than the thermal energy k_BT. This is known as a *Coulomb blockade* [63]. Here, two conditions are required to suppress electron transport. Firstly, the thermal energy must be significant smaller than the charging energy in order to avoid a blurring of quantized states ($k_bT < E_C$), and the tunnel resistance R_t must be sufficiently high, at minimum greater than the conductance quantum ($R_t > G_0 = \frac{h}{2e^2}$). Coulomb blockade manifests as a series

of sharp conductance peaks, with areas of zero or reduced conductance between, like in Fig. 2.11 (a).

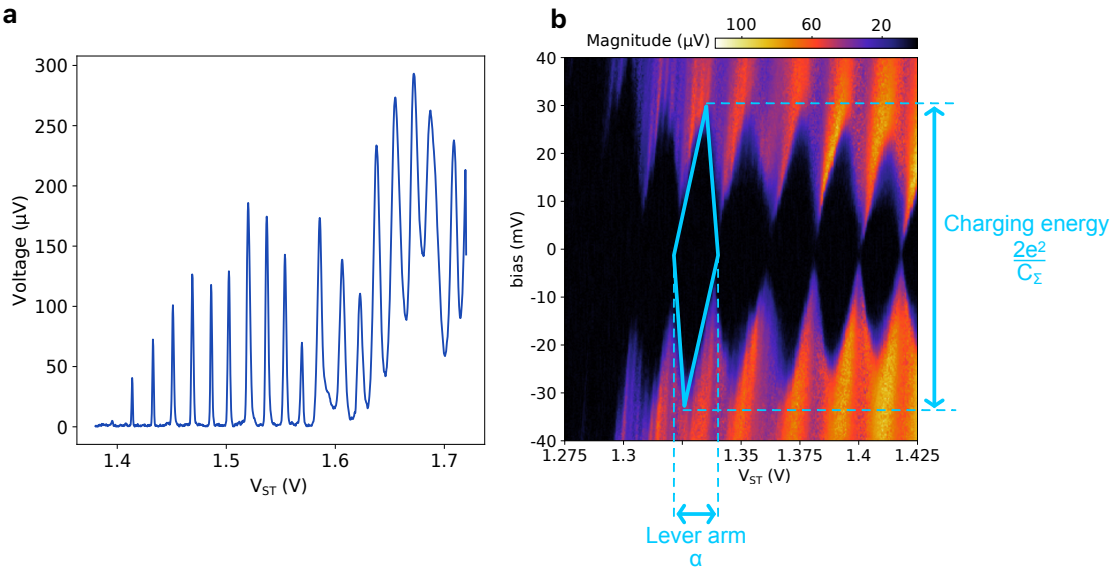

Figure 2.11: **Coulomb blockade and dot characteristics a,** Coulomb blockade through a single electron transistor. Current only flows when the electrochemical potential of the dot and the reservoirs align. **b,** Changing the bias across the reservoirs leads to Coulomb diamonds. The window in which conduction is allowed gets progressively larger as the voltage difference between the source and drain reservoirs increases, until Coulomb effects are no longer present. These diamonds reveal both the charging energy of the dot as well as lever arm α, a variable critical in calculating the electron temperature of samples.

Transport of electrons through a quantum dot only occurs within a *bias window*, when the electrochemical potential $\mu(N)$ of the dot is between that of the source and drain energy window:

$$\mu_s \geq \mu(N) \geq \mu_D \tag{2.26}$$

The amount of current flow is directly proportional to the bias window size, i.e. $\mu_d - \mu_s = eV_{SD}$ [63]. As the number of electrons in the dot repeatedly changes from N to $N+1$ and back to N in an ongoing cycle, a net current through the dot, I_{dot} is formed.

Single quantum dots are often utilized in readout applications, acting as an extremely sensitive charge sensor. Single electron transistors and sensing dots are common features on many quantum-dot devices, and readout techniques using them are detailed in Section 2.4.

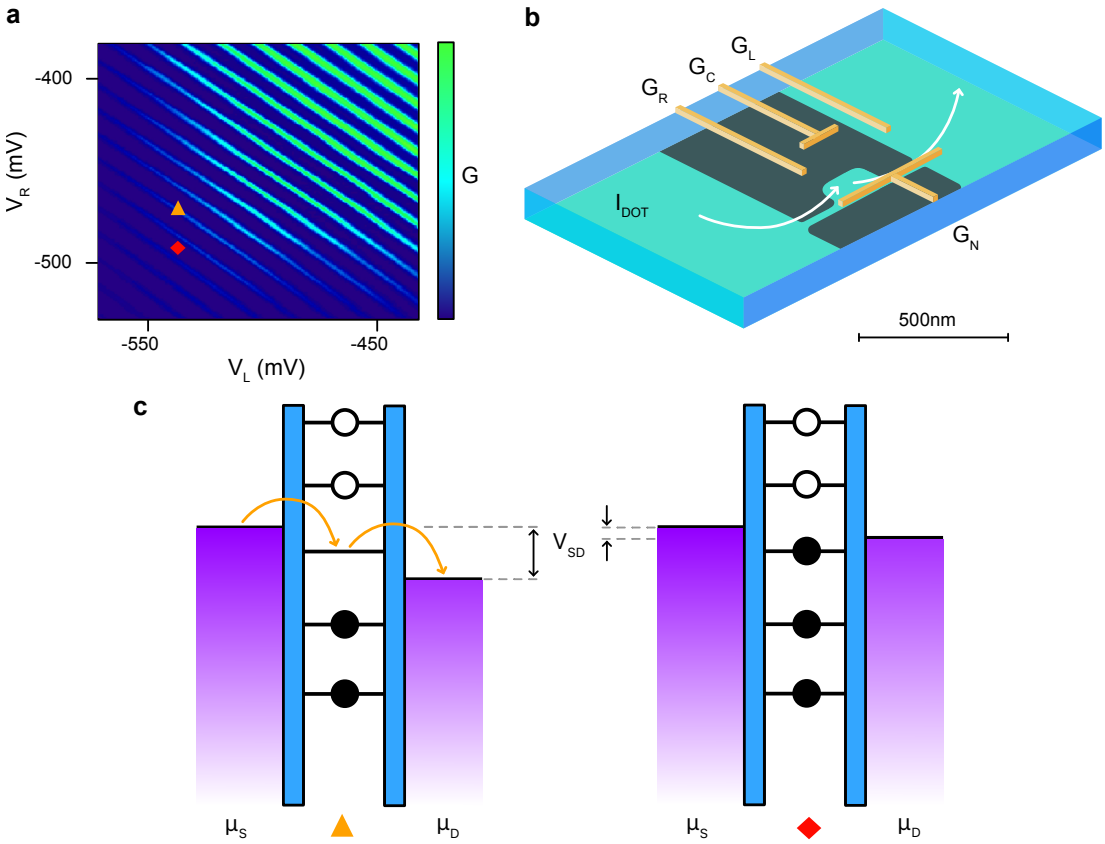

Figure 2.12: **Conductance through a single quantum dot. a,** The conductance is measured as a function of gate voltages V_R and V_L. The green stripes indicate regions where current is flowing through the dot within the bias window. **b,** A mock-up of what the defining gates for a quantum dot look like. A center gate with voltage V_C is primarily used for tuning the electrochemical potential of the dot, while all other gates are used for defining the dot in the 2DEG. The scale serves as approximation only, however single, double, and further multiple-dot systems in this thesis are of similar size. **c,** Illustration of transport through the quantum dot (left) and a Coulomb Blockade preventing transport (right). These regions correspond to light green (orange triangle) and dark blue (reg diamond) areas in (a) respectively. If the chemical potential $\mu(N)$ is within the bias window V_{SD}, electrons can travel on and off the dot as shown. Outside this window, no transport occurs as occupied levels are filled and unoccupied levels (or transport out of the dot) requires extra excitation of the charge carrier.

2.3.2 Double Quantum Dots

Leveraging superposition *and* entanglement in qubit systems detailed in this thesis requires double quantum dots. The addition of a second dot extends the analog of a single quantum dot as an artificial atom to a double quantum dot as an artificial molecule. Electron interactions between single quantum dots offer a distinct advantage over their single-dot counterparts, which is detailed in the next chapter. Our focus now, however, to examining how the addition of a second dot alters the prevailing interaction dynamics. In this scenario, the electrochemical potentials of the two dots are independently adjustable, while a tunnel barrier between them is modulated by an additional gate. The capacitive interaction between a dot and its nearest reservoir remains unchanged and resembles that of a single-dot system. Similarly, the capacitive coupling between the dot and the control gate electrode persists. The introduction of a second dot necessitates the introduction of new terms to account for the capacitive coupling between the two dots and the cross-capacitance between dots and opposing gate electrodes. The electrostatic potential of one of the dots becomes:

$$\mu_1(N_1, N_2) = U(N_1, N_2) - U(N_1 - 1, N_2) \tag{2.27}$$

$$= \left(N_1 - \frac{1}{2}\right) E_{C1} + N_2 E_{Cm} - \frac{E_C}{e}(C_S V_S + C_{1,1} V_{G,1} + C_{1,2} V_{G,2}) \tag{2.28}$$

$$+ \frac{E_{Cm}}{e}(C_D V_D + C_{2,2} V_{G,2} + C_{2,1} V_{G,1})$$

where $E_{C1(2)}$ is the charging energy of the individual dot, E_{Cm} is the electrostatic coupling energy, $C_{S(D)}$ is the capacitance between the dot and the source (drain), $C_{i,j}$ is the capacitance term between dot i and gate j, and $V_{G,1(G,2)}$ is the voltage on gate 1 (gate 2).

Unfortunately, the constant interaction model is limited in its approach to describe the tunneling dynamics between quantum dots. The *tunnel rate* between two quantum dots is an important metric that is not captured by this model. Carefully tuning the tunnel rate is important as it influences the performance of qubits. For example, high dot separation and a low tunnel rate may negatively impact the readout of these dots, and too high a tunnel rate leads to the gradual formation of a large single dot rather than a double-dot. I refer the interested reader to references [64], [65] and [66] for a more comprehensive overview on the topic.

Finally, the charge occupation, as well as the transport characteristics of a quantum double dot are visualized by *charge stability diagram*. In Fig. 2.13, (a) illustrates the capacitances and cross-capacitances experienced by each dot, while (b) showcases the energy levels enabling transport through the double dot under a source-drain bias. Each quantum dot harbors a discrete amount

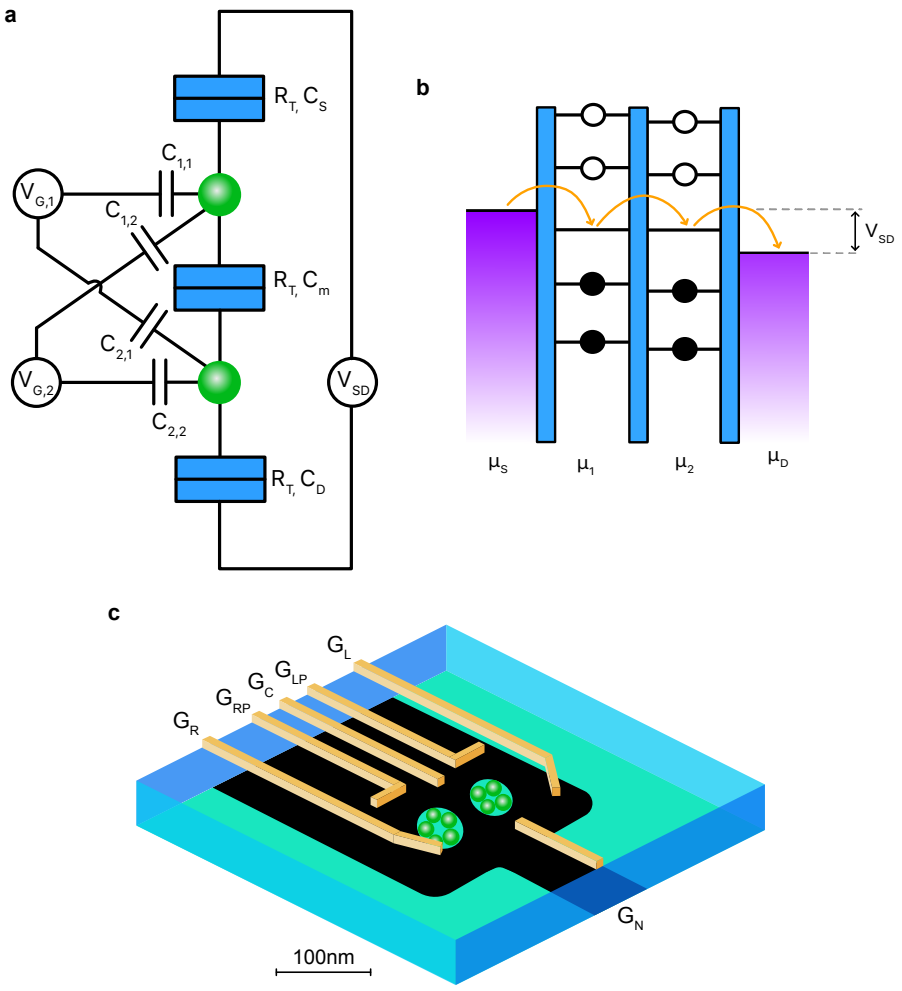

Figure 2.13: **Circuit diagram and current flow through a double quantum dot. a,** A circuit diagram representing capacitance and cross capacitance interactions between the dots, gates, and reservoirs. **b,** Transport through a double quantum dot. Transport is only possible when the energy levels of the two dots are within the bias window, or aligned with the source and drain chemical potentials. **c,** An illustration of gate confinement for a 2DEG double quantum dot. Similar to a single quantum dot, gates RP and LP modulate the electrochemical potentials of the two dots. The rest serve to confine the dots in two dimensions, close enough for entanglement interactions to be possible.

of charge, denoted as (n_1, n_2), where $n_{1(2)}$ signifies the number of electrons present. As additional capacitive and cross-capacitive terms are incorporated, the charge occupation evolves from a square grid as a function of gate voltages (Fig. 2.14 (a)) to a slanted grid (b), and ultimately to a honeycomb array (c). These transformations signify the influences of the gate electrodes on the opposing dots and inter-dot tunnel coupling, respectively.

Fig. 2.15 shows a detailed double-dot transition, visualizing the energy levels at particular areas

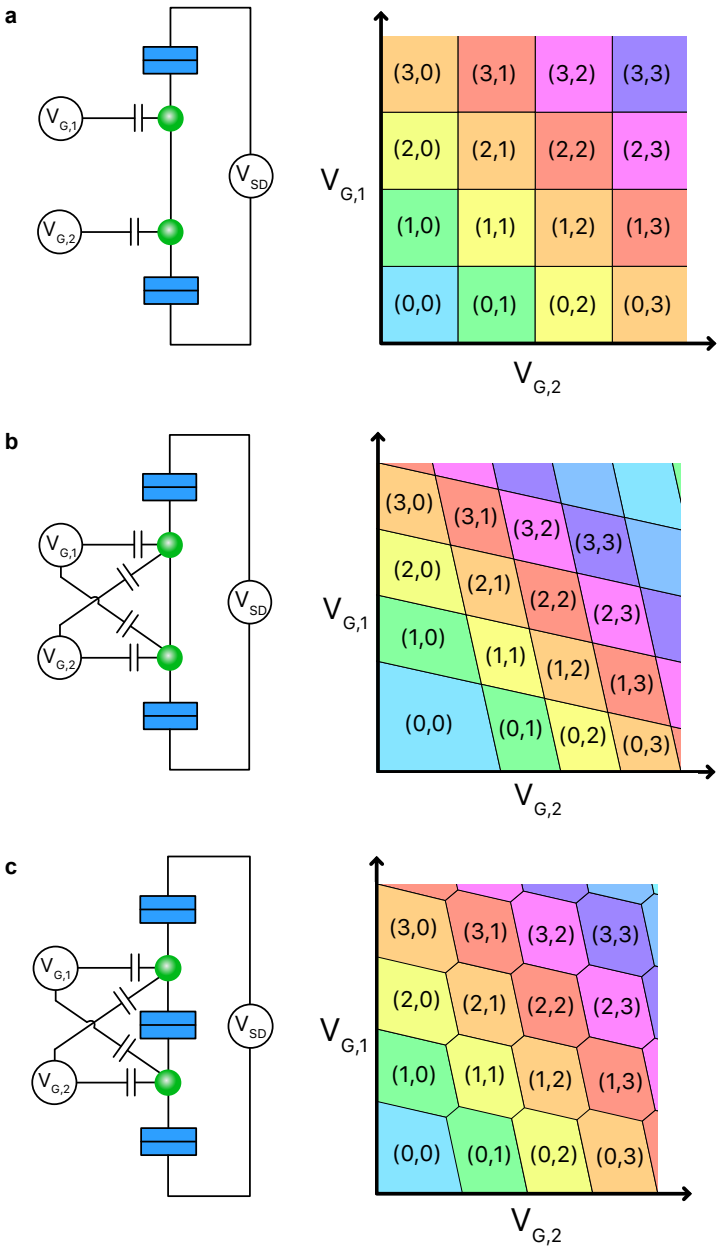

Figure 2.14: **Evolution of double dot stability diagrams. a,** The expected occupation picture if cross capacitance and inter-dot capacitance terms are not included. **b,** By including cross capacitance terms, the potential on one gate affects the opposite dot, leading to a sloping of the occupation squares in (a). **c,** Finally taking into account inter-dot interactions, inter-dot tunneling results in these splitting into hexagonal structures.

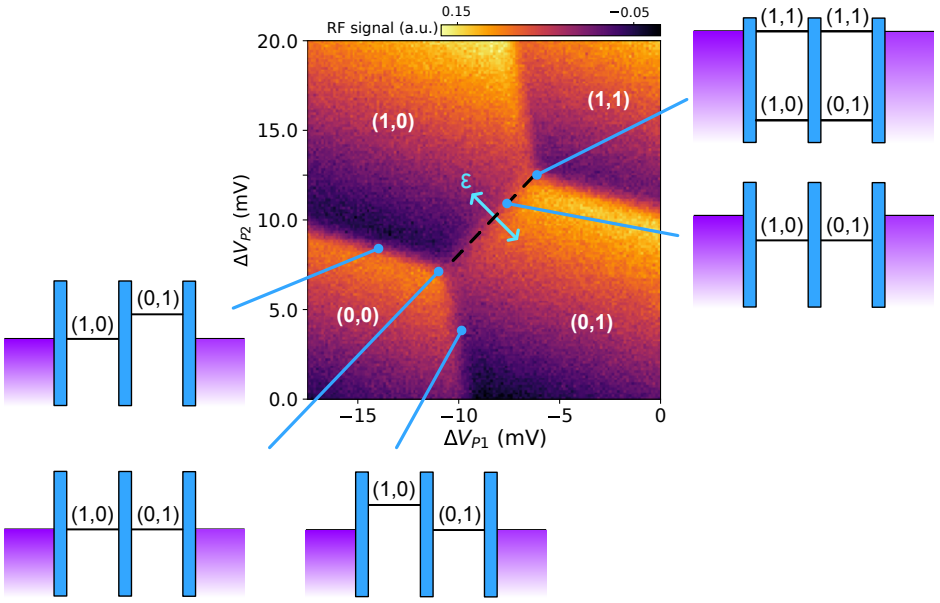

Figure 2.15: **Chemical potentials at various points on the charge stability diagram.** The alignment of certain chemical potentials is indicated at various charge transitions. Dot occupancies are indicated by the brackets. A new axis detuning ϵ is defined perpendicular to the inter-dot transition, a function of $V_{P1} - V_{P2}$.

of interest. Four dot-reservoir transitions are shown, indicating alignment of the reservoir chemical potential with one of the dots. The single inter-dot transition similarly indicates electrochemical alignment of the two dots. Triple points represent instances where the electrochemical potential of the two dots and reservoirs converge, thereby permitting current flow through the dots. If, for example, the left reservoir is considered the source, then populating the right dot with a single electron may follow the following sequence: align the left dot and source chemical potentials to load a dot in, i.e. (0,0) $\rightarrow$ (1,0). Then, change the chemical potential of the left dot to match the right, and then raise it above the right to promote the electron to move (1,0) $\rightarrow$ (0,1).

Isolated Quantum Dots

Up to this point, the discussion has revolved around quantum dots coupled to an electron reservoir. In realizing a million-plus qubit system however, this setup becomes impractical, as the vast majority of dots will lack a direct connection to a reservoir. In fact, two-qubit systems today operate in what is termed as the "isolated mode" configuration, where dots function independently without direct reservoir coupling. In Chapter 5 for example, qubits are operated within an isolated double dot setup, wherein the tunnel barrier between the dots and reservoir is elevated. This de-

parture from the traditional double dot configuration eliminates the reservoir-dot capacitive terms, resulting in charge stability diagrams featuring only inter-dot transitions, see Fig. 2.16 (b).

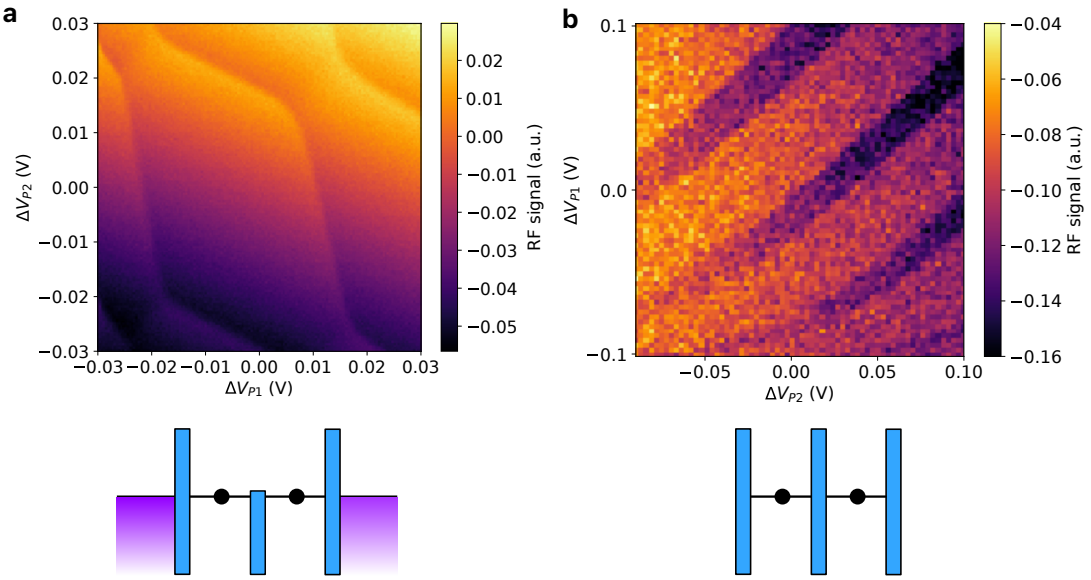

Figure 2.16: **How gate tuning changes charge stability diagrams. a,** By lowering the potential barrier between the two dots, the interdot transitions become blurred as the two dots start to join into one. **b,** By isolating double dots from the reservoirs, only inter-dot transitions remain. Isolated double dot stability diagrams are commonly a function of detuning ϵ and tunnel coupling.

2.3.3 Electron Occupancy: Orbital and Valley Splitting

In silicon systems, 2DEGs introduce additional complexities to the quantum dot landscape. Throughout this chapter, the figures predominantly showcase transitions with a total electron count of two, representing the most simplistic and commonly operated regime. Chapter 5 , however, explores a Si double-dot device with a total electron occupancy of four. This divergence arises from the disparity between valley (one electron per dot) and orbital (multiple electrons per dot) energy splitting, with the latter offering advantages for qubit operations.

In bulk silicon, the conduction band contains six energy minima called *valleys*. The valleys are degenerate, but this degeneracy is lifted in nano-scale qubit devices due to sharp material interfaces (Si/SiO_2) and application of electric fields [67, 68]. Two degenerate ground states and four degenerate excited states are further lifted by the surface strain at the Si/SiO_2 interface. Valley states are tunable [69], which is crucial to operation of qubits in such a state in order to maximise energy splitting.

Moreover, the addition of extra electrons within a quantum dot reveals a well-defined shell structure. The orbital energy splitting tends to be larger than the valley splitting and is tunable via confinement potential, on the order of > 2.5 meV, versus > 500 μeV for valley splitting [70]. Higher electron occupancy also exhibits advantages with faster Rabi driving and higher Q factor ($Q = T_2^{\text{Rabi}}/T_\pi$) [71].

These relatively high valley and orbital splitting levels allow for the operation of qubits above 1 K [35, 72], a crucial factor enabling the scalability of large qubit arrays. The operation at these temperatures allows for the accommodation of more "hot qubits" within a single dilution unit, owing to increased cooling power.

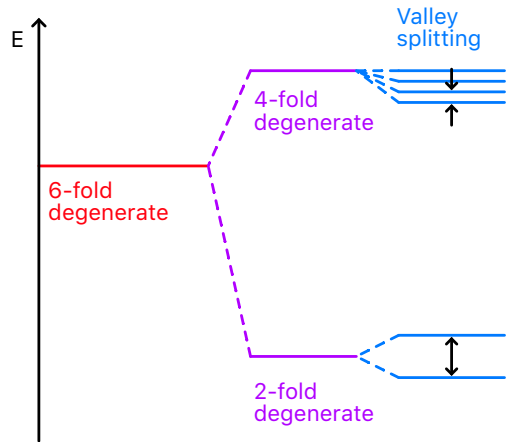

Figure 2.17: **Valley splitting in the bulk silicon substrate.** At the interface of Si and SiO_2, the six-fold degenerate valley degeneracy is broken. The remaining two- and four-fold degeneracies are broken by electric fields and tight confinement.

2.4 Readout

A single electron tunneling into a quantum dot constitutes a tiny change in the local environment, necessitating extremely sensitive charge probes for detection. The probes must not impede the ability to scale the qubit systems, *and* complete the readout process on microsecond timescales, faster than the lifetime of the qubits. These requirements have lead to innovative approaches such as exquisitely sensitive proximally placed charge sensors, *in-situ* gate probes, the adoption of high bandwith radio-frequency technology, and novel techniques to discriminate between electron spin states. This section details the aforementioned readout techniques, integral to the experimental outcomes in Chapters 4 and 5.

2.4.1 Charge Sensors

Quantum point contacts and single quantum dots serve as highly sensitive charge sensors when positioned near quantum systems. The realisation of these discrete structures increases readout complexity, and requires careful consideration of trade-offs in sensitivity and scalability as part of the entire quantum system. Two popular readout structures are quantum point contacts and single electron transistors. I've covered the physics of both already, in sections 2.2 and 2.3 respectively. Here, I examine the benefits of both systems, in the context of their sensitivity and suitability in GaAs or silicon systems.

Quantum Point Contacts

The width of a one-dimensional conductance channel is highly sensitive to changes in its surrounding environment [73, 74]. Tuned into the right regime (see Fig. 2.18), at the steep quantized conductance transition, these small channel width modulations result in a significant change in the readout signal. The quantum point contact (QPC) demonstrates remarkable sensitivity, capable of detecting single-electron loading and unloading events within quantum dots, as well as inter-dot transitions. An electron tunneling on or off a nearby quantum dot shifts the electric field in the surrounding areas, changing the QPC channel width. A small shift in the quantized steps with respect to gate voltage results in a large change in the conductance in the channel. The exact shape of quantized steps changes with device geometry. Typically, the first quantized step is the most sensitive point (steepest change in conductance), however for stability occasionally the second or third quantized step is used instead.

Single Electron Transistors

The single electron transistor (SET) [75, 76] is another name for a single quantum dot often used for readout. Similar to the dynamics of a QPC, a single electron transistor is tuned to the most sensitive point–one of the edges of a Coulomb peak (within a Coulomb blockade regime). SETs are more popular in many architectures compared to QPCs, both due to their ease of construction[1] and increased sensitivity. SET sensors are up to 30 times more sensitive than QPCs, due to differences in both the conductance slope and screening effects. I point the interested reader to reference [77] for more details.

Construction of an SET is shown in Fig. 2.19. This particular SET is based on a silicon-metal-oxide-semiconductor (SiMOS) architecture, where a sufficiently positive gate voltage allows for

[1] In silicon systems for example, a 2DEG is defined by applying a positive voltage to a gate on the surface. Tunability of a QPC, therefore, would likely require the same number of gates as an SET with less sensitivity.

electron conduction. One gate is connected to two ohmics, that provide an electrochemical bias and electron reservoir. This gate overlaps with two barrier gates that define the quantum dot necessary for achieving sensitivities capable of detecting single-electron events. Unlike qubit-specific quantum dots, SETs are often tuned to higher electron occupancy numbers (on the order of 10s to 100s) to achieve greater sensitivity.

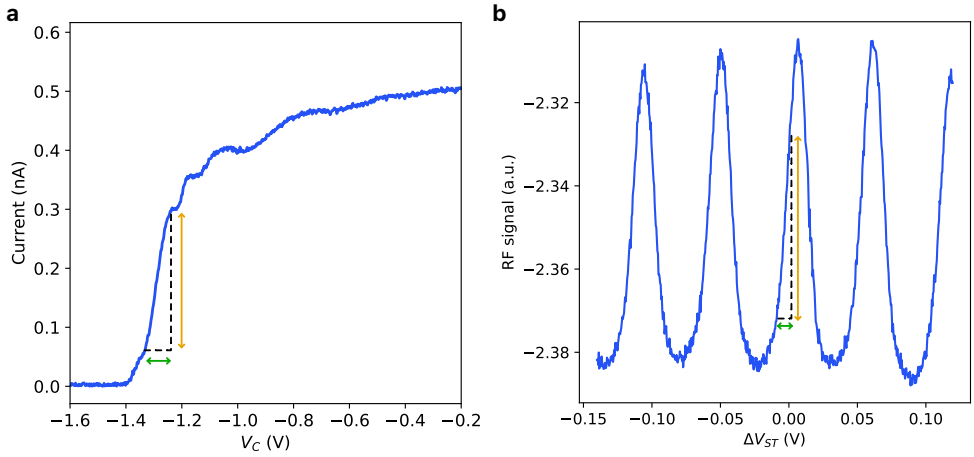

Figure 2.18: **QPC and SET charge sensing. a**, Conductance through a QPC channel as a function of gate voltage. A small shift in the channel relative to gate potential (green arrow) leads to a large change in measured conductance. **b**, SETs work under a similar mechanism, exploiting the fast conductance rise of the coulomb blockade.

2.4.2 Radio-Frequency Reflectometry

The speed at which a quantum state is measured is extremely important. The maximum readout period for any qubit is limited by T_1 lifetime[78, 79]. Exceeding this results in a signal that is not representative of the qubit state [80]. Reduction of readout time is possible using a radio-frequency reflectometry technique, leveraging much higher bandwidths through integration of the readout sensor into an impedance matching network [81–84]. RF reflectometry measures the reflectance of a high frequency signal sent down the circuit. The nature of the reflected signal changes in step with changes within the quantum system. The advantage is the speed of readout, and compatibility with existing readout structures.[1] QPCs and SETs can be used for traditional DC charge sensing and RF reflectometry. RF sensing achieves sensitivities of $30\,\mu v/\sqrt{Hz}$, [87, 88] and benefits from cryogenic low noise amplification that improve signal-to-noise ratio.

[1] This is extremely important in more complex quantum circuits that utilize ancilla qubits [85, 86]. And from a practicality standpoint, an experimentalist is far more productive if total measurement time is an hour vs. a week, able to iterate and explore the parameter space in far more detail over the same period.

Impedance Matching

In order to effectively read out a quantum state, the characteristic impedance of a quantum device and readout circuit need to be matched. If not, the big impedance mismatch results in almost 100% of the transmitted signal being reflected, resulting in negligible sensitivity. This impedance mismatch occurs at the junction of two mediums with dissimilar characteristic impedances. Naively connecting a coaxial transmission line directly to a quantum sensor would lead to a significant mismatch, as the characteristic impedance of the transmission line is $Z_0 = 50\ \Omega$, much less than that of the sensor on the order of:

$$Z_{\text{load}}(\omega) = \frac{1}{\frac{1}{R_{\text{load}}} + j\omega C_p} \tag{2.29}$$

where $R_{\text{load}} \sim 25\ k\Omega$ and $C_p \sim 1$ pF. The reflection coefficient is a ratio between incident and reflected waves:

$$\Gamma(\omega) = \frac{Z_{\text{load}}(\omega) - Z_0}{Z_{\text{load}}(\omega) + Z_0} \tag{2.30}$$

Clearly $Z_{\text{load}} \gg Z_0$, such that nearly all incident signal is reflected resulting in negligible sensitivity to changes in the sensor.

By embedding an inductor into the matching network, the high impedance of the charge sensor is transformed towards that of the transmission line at a particular resonant frequency [89]. The existing parasitic capacitance in conjunction with the resonator has an impedance of:

$$Z_1(\omega) = Z_L(\omega) + Z_{\text{load}}(\omega) = j\omega L + \frac{1}{\frac{1}{R_{\text{load}}} + j\omega C_p} \tag{2.31}$$

which equates to:

$$Z_1(\omega) = j\omega L + \frac{1}{j\omega C_p} + R_{eff} \tag{2.32}$$

where:

$$R_{eff} = \frac{1}{R_{\text{load}}}\left(\frac{L}{C_p}\right) \tag{2.33}$$

The impedance matching network is shown in Fig. 2.19, and consists of lumped element superconducting niobium spiral inductors on a sapphire substrate in series with a capacitor, a parasitic capacitance, and dynamic resistance of the quantum sensor [9]. The choice of inductor value (typically 50 nH to 1000 nH) determines the frequency at which matching occurs, i.e. $\Gamma = 0$ and

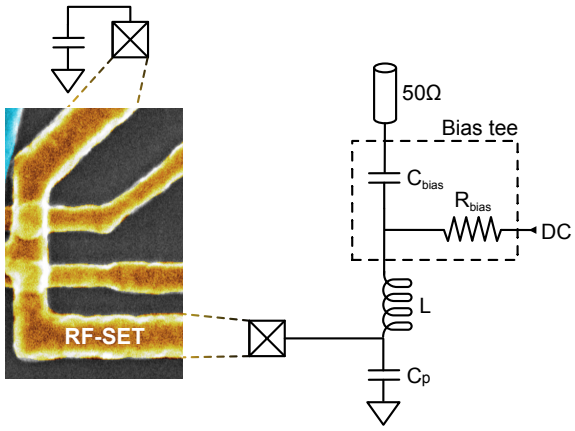

Figure 2.19: **Impedance matching network.** An inductor and capacitor are placed in series with the SET resistance, change the impedance to better match the characteristic 50 Ω transmission line. A bias tee is included, as ohmic contacts often require a voltage bias for measurement purposes.

$R_{eff} = 50\ \Omega$. The matching condition is illustrated in Fig. 2.20, where a shift in Z_{load} results in a large change in reflected signal near the impedance matching condition, and close to no change far from this condition.

Dispersive Gate Sensing

SETs and QPCs are discrete elements that add complexity, especially at high qubit counts. The requirement that these charge sensors be placed close to the qubits necessitates multi-layer gate fabrication in anything other than small qubit arrays [14, 90], and the extra on-chip space needed increases the number of long-distance coupling mechanisms between arrays of qubits. An alternative approach, using RF techniques, leverages the capacitive coupling of an *in-situ* gate electrode to probe capacitive changes in the surrounding environment. The reduced readout complexity at large qubit numbers leads to a scalability advantage that has prompted multiple experiments to explore this technique in semiconducting systems [91–93]. The probe gate often defines a quantum dot, meaning proximal SETs are no longer required. This sensing technique retains similar sensitivity to SET-based readout, enabling fast single shot readout times of qubits [31, 88, 94].

Dispersive gate sensing (DGS) embeds the gate electrode into a lumped element circuit to probe LC shifts of single electron charge transitions. This system is approximated as a series RLC circuit, with a parasitic capacitance C_p parallel to the system capacitance C_s, see Fig. 2.21. Resonance occurs when the inductive and capactive terms are equal $j\omega L = 1/(j\omega C_p)$, such that:

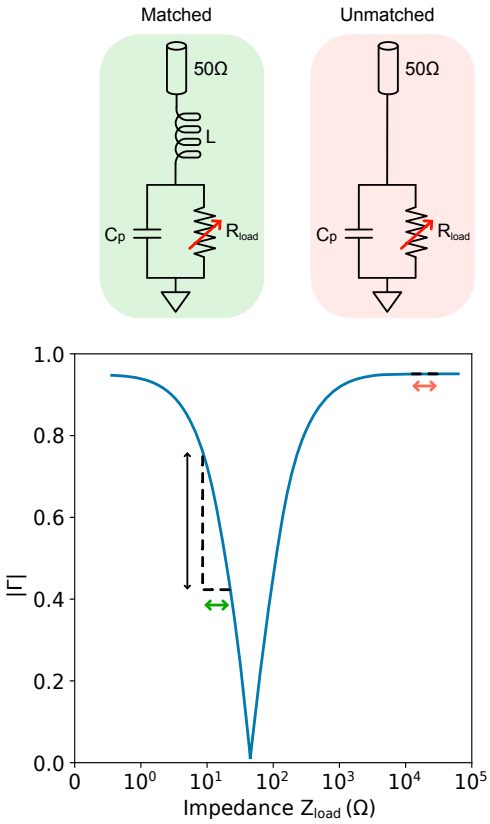

Figure 2.20: **Impedance matching behaviour.** Calculated reflection coefficient as a function of lumped element impedance. At well-matching regimes, small changes to the load resistance leads to a large change in reflected signal. In unmatched regimes, negligible change in reflected signal is observed.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.34}$$

The capacitive term comprises both parasitic and quantum capacitance $C = C_p + C_q$.

Demodulation

To extract information from the reflected wave, it's necessary to demodulate the signal into magnitude and phase quantities. Initially, a carrier wave is split at room temperature into *incident* and *reference* signals. The incident signal travels down the cryogenic fridge, passes through a directional coupler, and encounters the quantum device's impedance, causing partial reflection. The reflected signal then makes its way back up through the fridge, where it's amplified at 4K before continuing towards a mixer at room temperature. Meanwhile, the reference signal acts as the local

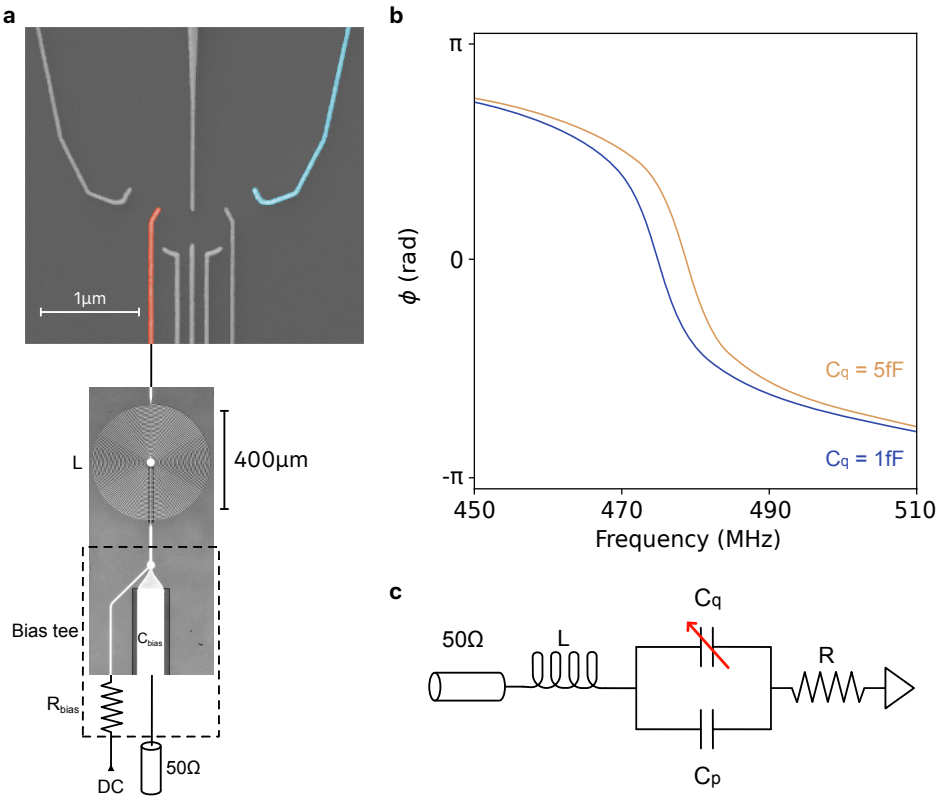

Figure 2.21: **Dispersive sensing. a**, Dispersively sensing a signal using an *in-situ* gate. A microscope image of the lumped-element LC resonator is included. **b**, Phase response of a reflected signal as a function of frequency. At a well-matched point, changes in the quantum capacitance lead to a large phase change of the reflected signal. **c**, Equivalent circuit of a dispersively sensed load. Instead of a resistance, changes in the device's quantum capacitance leads to magnitude and phase changes in the reflected signal.

oscillator (LO). It's mixed with the reflected signal during demodulation, resulting in a combined signal whose amplitude is dependent on the amplitude and relative phase of both the incident and reflected signals. For a visual representation of this demodulation process, refer to the RF setup schematic shown in Fig. 2.22. Both incident and reflected waveforms are characterized by a combination of amplitude A and phase φ.

$$V_I = A_I \cos(\omega t + \varphi_T) \tag{2.35}$$

$$V_R = A_R \cos(\omega t + \varphi_R) \tag{2.36}$$

where A_I and A_R are the incident and reflected signal amplitudes respectively, φ_I and φ_R are the

respective phases, and ω is the carrier frequency. By mixing the transmitted and reflected waves, the amplitude A_R and phase φ_R information is extracted such that:

$$V_{IF} = V_I \times V_R \tag{2.37}$$

$$= \frac{1}{2} A_I A_R (\cos(2\omega t + \varphi_I + \varphi_R) + \cos(\varphi_I - \varphi_R)) \tag{2.38}$$

The high frequency components are filtered out, leaving only a DC component:

$$A_I A_R \frac{1}{2} \cos(\varphi_T - \varphi_R) \tag{2.39}$$

This demodulation process does not preserve phase information. However, by repeating demodulation with a second reference tone and a 90° offset, magnitude and phase can be calculated using trigonometric identities.

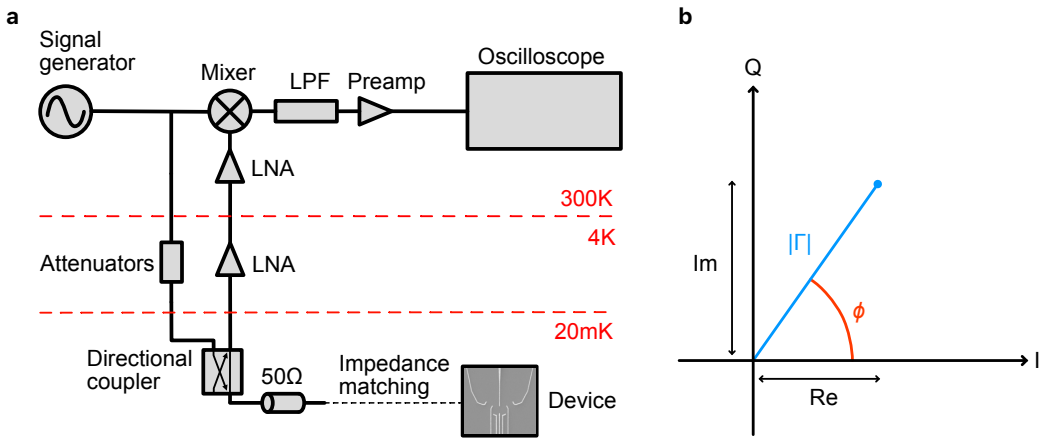

Figure 2.22: **Demodulation circuit. a**, A full demodulation circuit for the readout of a generic quantum device. A carrier signal is generated a room temperature and is split, with one half travelling down the fridge to the device. Attenuators reduce the noise temperature to acceptable levels for the device. The reflected signal is routed through a directional coupler and amplified before being low pass filtered and mixed with the LO signal before sampling. **b**, Demodulation represented as components of in-phase (I) and quadrature (Q) signals. The absolute magnitude and phase are extracted as shown.

2.4.3 Readout of Spin Qubits

Measuring the spin state of a qubit requires a spin-to-energy conversion via a spin-dependent process. Various techniques have been developed to achieve this, such as spin-resolved spectroscopy

[95], spin-dependent tunneling [96], transport measurements [97], optical methods [98], and more. However, each technique requires sophisticated sensors and comes with tradeoffs in terms of sensitivity, speed, complexity, and compatibility with other qubit systems. Today, silicon qubit spins for large-scale quantum computers are often detected via a spin-to-charge conversion, whereby an electron's spin determines the probability of a tunneling event. This is an energy dependent mechanism, exploiting the spin energy splitting at high magnetic fields. SET's are often used as the detection probes[99–106].[1] This section delves into the readout techniques associated with spin qubit dynamics, complementing the discussion on the physics of spin qubits, particularly singlet-triplet qubits, detailed in Chapter 3.

The physics of spin-to-charge conversion is illustrated in Fig. 2.23. In a magnetic field, Zeeman splitting acts to separate electron energy levels dependent on spin state. When this splitting is higher than the thermal excitation energy, spin-selective tunneling can occur, called *Pauli spin blockade*. A source-drain bias is applied to straddle the energy levels of the two dots. An electron of any spin state can enter the left dot forming either a singlet or triplet (1,1) state, which are nearly degenerate [108]. The right dot, however, can only accept a (1,1) singlet state due to the higher energy level of the triplet (0,2) state. Consequently, occupation of the triplet (1,1) state prevents further transport due to conservation of spin [109]. Under opposite bias, current flows since the singlet (0,2) state has a higher energy than the singlet (1,1) state. Electrons cannot form a triplet (0,2) state due to the higher energy level.[2]

Pauli spin blockade is observed at higher electron occupancies too. Inter-dot transitions with a total electron number that is odd do not exhibit spin blockade behavior. For those with an even number, one charge state (say [2,2]) forms a singlet ground state, while the the other ([1,3] or [3,1]) forms a singlet or triplet state. Fig. 2.23 (c) details inter-dot transitions where spin blockade occurs.

Readout of spin qubit states introduces a new concept of *visibility*, which represents a function of both initialization and readout fidelity. In an ideal scenario, where the device operates flawlessly, measured spin states are pure, being fully blockaded or fully unblockaded. In this perfect setup, there are no control or readout mechanisms contributing to qubit preparation errors or inducing spin flipping. In the real world of experimental settings, however, the Pauli spin blockade is partially lifted by various processes. These include thermal excitations that elevate electrons beyond the energy deficit between the $(0, 2)$ and $(1, 1)$ charge states [111], as well as mechanisms that induce state mixing between spin states. Such mixing is often caused by phenomena like co-tunneling

[1] Dispersive readout with such systems is also possible, utilizing *in-situ* gates [93] or a single electron box [107] (very similar construction to an SET), but this is beyond the scope of this thesis and not relevant to this discussion.

[2] In some cases, $|T_0\rangle$ spin state relaxes quickly to the singlet state, blockading only the $|T_+\rangle$ and $|T_-\rangle$. Here, discrimination occurs between even and odd spin parity, known as *parity readout* [110].

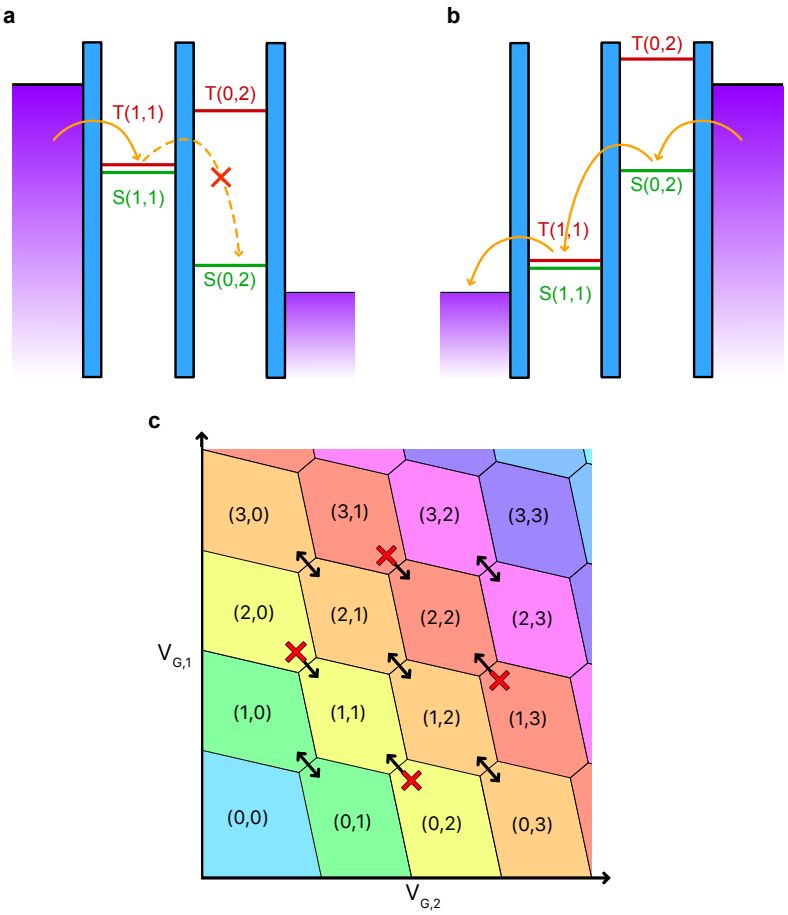

Figure 2.23: **Pauli spin blockade. a**, Transport of triplet states is fully suppressed due to the spin blockade as the T(0,2) state has a higher energy. Singlet states are still allowed to transport across. **b**, Singlet electrons are free to transport across the double dot due to the permitted energy levels. The source-drain bias levels mean triplet states are not loaded. **c**, Spin blockade at higher electron occupancies. Blockade only occurs when the total electron number is even.

[112, 113], hyperfine interactions [114–116], and spin-orbit interactions [117, 118]. It's crucial to mitigate these factors to enhance visibility and overall device performance.[1]

[1] Multiple control techniques must also be implemented to improve visibility, for example [35].

3

Quantum Operations with Qubits

In Chapter 1 we examined the requirement for a qubit to be formed from a system exhibiting individually addressable two-level-like behavior. While the principles of quantum mechanics offer abundant candidates for such systems, the challenge lies in harnessing any particular two-level system while maintaining a scalable approach. Among the array of options, spin-based systems have unique advantages, rendering them ideal for large-scale qubit systems. Spin qubits exhibit relatively long coherence times, are easily controllable, and have minuscule physical footprints, enabling the potential placement of thousands or millions, of qubits on a single die, before necessitating long-distance coupling. Some spin-based qubit architectures also have the advantage of being relatively straight-forward to create: trap an electron in a magnetic field, and Zeeman splitting creates two distinct energy levels contingent upon the spin of the electron.

Spin principally serves as the cornerstone of quantum information processing due to its accessibility and resilience against certain noise sources. However, the manner in which spin is utilized to encode qubits varies across platforms, necessitating trade-offs that aim for long-term advantages [119–121]. The architectures that leverage spin qubits to build scalable qubit systems include: single spin [122, 123], singlet-triplet [35, 111, 124], donor-based [125–128], and exchange systems [129–134]. This chapter examines single spin and singlet triplet systems, while briefly touching on other qubit architectures relevant to discussion.

3.1 Qubit Encodings

The previous chapter introduced the physics of quantum systems and showed how a two level system that satisfies the Loss-DiVincenzo requirements is built. Quantum dots, for example, explored in Section 2.3, are an effective means of elucidating the quantized nature of electrons. We can encode qubits within quantum dots by assigning the two energy levels to the poles of the Bloch sphere. How this is realized in practice changes depending on the *kind* of qubits we choose to encode. The following subsections detail important qubit encodings relevant to discussion in this thesis. It is important to note that the following descriptions of different spin systems are not exhaustive, and readers are encouraged to consult the references provided for more comprehensive overviews [135–138].

3.1.1 Charge Qubits

One of the simplest ways to create a qubit involves manipulating the charge distribution between two sites, termed a charge qubit. In this scheme, a single electron occupies either the left or right quantum dot, with the charge state of the quantum dot encoding quantum information. Specifically, $(0,1) = |0\rangle$ and $(1,0) = |1\rangle$, where $|0\rangle$ and $|1\rangle$ correspond to electrochemical potentials E_0 and E_1, respectively.

This type of qubit is highly susceptible to charge fluctuation noise. Decoherence induced by random charge fluctuations drastically reduces coherence times to a mere 10 ns, rendering them operationally impractical in building a useful quantum computer [139].

3.1.2 Single Spin Qubits

Spin qubits offer advantages over their charge qubit counterparts as they are less sensitive to charge noise, possessing longer coherence times for a greater number of operations before decoherence. The spin of an electron emerges as an ideal candidate for a qubit due to its inherent two-level nature, prolonged coherence time, and easy realization within quantum dots. In this configuration, quantum information is encoded onto the spin state of an electron confined within a quantum dot, with spin up $|\uparrow\rangle$ corresponding to the state $|0\rangle$ and spin down $|\downarrow\rangle$ representing $|1\rangle$. Energy levels are split by an amount $E_Z = g\mu_B B$ where g is the g-factor and μ_B is the Bohr magneton.

Single-qubit control is achieved through the manipulation of a oscillating magnetic and electric fields. Various techniques exist for generating these fields including electron spin resonance (ESR) [140] and electron-dipole spin resonance (EDSR) [141]. Devices within this thesis predominantly

utilize electron spin resonance, a method elaborated upon in greater detail in Section 3.2.2.

3.1.3 Singlet-Triplet Qubits

A simple extension from the single spin qubit is the singlet-triplet qubit. This architecture relaxes some of the requirements of single spin qubits, namely the use of oscillating electric or magnetic fields for control, and is more insensitive to magnetic noise. A singlet-triplet qubit leverages the interaction between two spins to form a single qubit, regulated by a combination of coupling energy $J(\epsilon)$ and Zeeman energy splitting. Control in this framework predominantly involves baseband gate pulses, which reduce input-output complexity and power consumption, especially at large qubit numbers. Additionally, this electric-field-based approach is easier for precise control compared to oscillating fields. The two-level system is formed by the energy splitting between the singlet-triplet $|S\rangle$ and $|T_0\rangle$ states, encoding as $|0\rangle$ and $|1\rangle$ states respectively. To minimize the probability of leakage, a global static magnetic field is applied due to the degeneracy of the T_0 state with the T_+ and T_- states.[1]

Expanding the singlet-triplet basis to two qubits results in the creation of multiple states:

$$|\uparrow\uparrow\rangle\,,\ |\uparrow\downarrow\rangle\,,\ |\downarrow\uparrow\rangle\,,\ |\downarrow\downarrow\rangle \tag{3.1}$$

The four possible spin states of this system are:

$$\begin{aligned} |S\rangle &= |0,0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle) \\ |T_-\rangle &= |1,-1\rangle = |\downarrow\downarrow\rangle \\ |T_0\rangle &= |1,0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle) \\ |T_+\rangle &= |1,1\rangle = |\uparrow\uparrow\rangle \end{aligned} \tag{3.2}$$

Like their single spin counterparts, singlet-triplet systems suffer from noise processes that decrease coherence times. Notable noise sources affecting spin-qubit systems include local magnetic fluctuations, variations in the g-factor, impurities leading to random spin-orbit coupling, and two-level fluctuators contributing to charge noise. Mitigation of this noise through various protocols is an active area of research [142–146].

[1] If the states are degenerate, then we may inadvertently initialize into a T_- or T_+ state with different spin properties, negatively impacting subsequent operations on an assumed T_0 state.

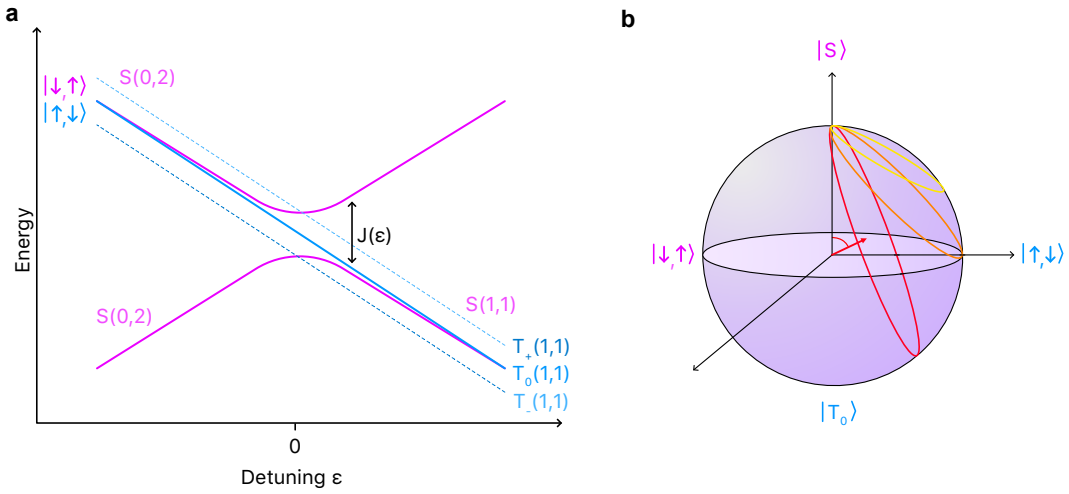

Figure 3.1: **Singlet triplet energy states.** **a**, Singlet triplet states as a function of detuning and energy. Tunnel coupling, magnetic field are both non-zero, leading to avoided crossings and Zeeman splitting of the T_+ and T_- states. A S(0,2) state indicates a singlet state with a (0,2) electron occupation in the quantum dots. **b**, Qubit rotations corresponding to the $S - T_0$ transitions. Rotations change as a function of detuning ε and pulse duration [147].

3.1.4 Majorana Zero Modes

Finally, we turn to Majorana zero modes (MZMs), an alternative qubit platform promising protection from local noise for much higher qubit fidelities [148], and serving as a key motivator for the experiment discussed in Chapter 4. MZMs utilize non-abelian anyons within a degenerate ground state, wherein quantum information is stored in pairs of anyons distributed over a macroscopic distance. This configuration renders the system resistant to local noise sources such as charge fluctuations, which commonly afflict spin qubit platforms. Only by braiding these anyons can the system undergo more sophisticated evolution required for quantum algorithms. Theoretically, the qubit fidelity of this system surpasses that of other qubit architectures, facilitating a lower physical qubit count for every logical qubit and enhancing scalability.

Creating these quasiparticles demands a highly specific setup. Kitaev proposed a one-dimensional chain of fermions governed by the following Hamiltonian [149]:

$$H = \sum_j \left(-w(a_j^\dagger a_{j+1} + a_{j+1}^\dagger a_j) - \mu(a_j^\dagger a_j - \frac{1}{2}) + \Delta a_j a_{j+1} + \Delta^* a_(j+1)^\dagger a_j^\dagger \right) \tag{3.3}$$

where $a_j, a_j^\dagger$ are the annihilation and creation operators respectively, w is the hopping amplitude, μ is the chemical potential, and Δ is the superconducting gap. From here, the Majorana operators are:

$$c_{2j-1} = a_j + a_j^\dagger, \quad c_{2j} = -i(a_j - a_j^\dagger) \tag{3.4}$$

Rewriting the Hamiltonian in terms of these operators becomes:

$$H = \frac{i}{2} \sum_j (\mu c_{2j-1} c_{2j} + (w + |\Delta|) c_{2j} c_{2j+1} + (-w + |\Delta| c_{2j-1} c_{2j+1}) \tag{3.5}$$

The tuning of the system, dependent on w, μ, and Δ, dictates whether Majoranas form pairs as part of a single particle, or as pairs across different particles. The first case, where $|\Delta| = w = 0, \mu < 0$, sees Majorana pairs form within a single fermion. The Hamiltonian from this situation

$$H_{\text{trivial}} = -\mu \frac{i}{2} \sum_j c_{2j-1} c_{2j} \tag{3.6}$$

shows the Majorana operators present c_{2j-1} and c_{2j} come from the same site j. The non-trivial situation, where $|\Delta| = w > 0$ and $\mu = 0$ has a different Hamiltonian

$$H_{\text{nontrivial}} = iw \sum_{j} c_{2j} c_{2j+1} \tag{3.7}$$

with Majorana operators from different sites.

A comprehensive description of Majorana modes and all its possibilities would merit an entire thesis in itself. I direct the reader towards the following material for further insight [150][151][152].

At present, fabricating Majorana-based qubits remains a formidable challenge [153–156]. Qubit fidelities have yet to be established, and it remains unclear whether the considerable increase in construction complexity of a single qubit will yield a proportionate long-term advantage over its spin-qubit counterparts.

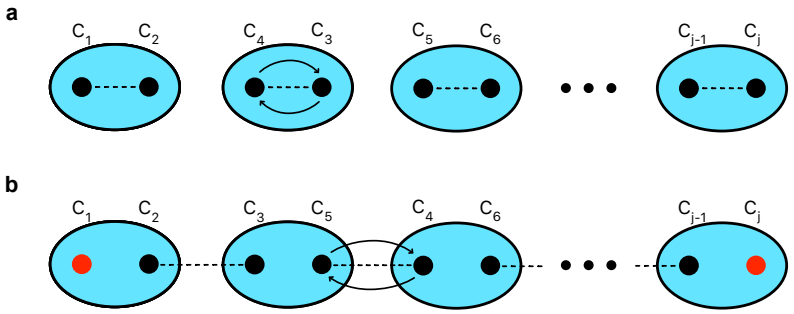

Figure 3.2: **A Majorana zero mode. a**, Pairing of Majorana zero modes under the trivial case H_{trivial}. The pair (c_3, c_4) have been swapped, corresponding to an abelian exchange. In reality, these Majoranas cannot be manipulated individually under this condition. **b**, Pairing of Majorana zero modes under the second case $H_{\text{nontrivial}}$. Once again, a pair (c_4, c_5) has been swapped. Since pairing is between particles, however, this becomes a non-abelian exchange. The two extreme Majoranas c_1 and c_j are unpaired. Making use of these unpaired states correctly promises a qubit robust to local noise fluctuations.

3.2 Features of a Single Spin Qubit

Understanding the behavior of single qubits is fundamental to the scale-up of large quantum systems. Intrinsic properties, environmental contributions, and controlability collectively shape a qubit's ultimate performance. Although the introduction of additional qubits complicates the landscape, many of these factors retain their significance in determining the error rate of the system.

The rest of this chapter is focused primarily on the realisation of singlet-triplet qubits, however aspects are generalizable to other systems. This section covers intrinsic behaviors of single spin qubits, before exploring control operations, coherence, and characterization of qubit performance.

3.2.1 Larmor Precession

When subjected to an applied magnetic field, an electron's magnetic moment naturally undergoes precession. This phenomenon holds particular relevance for qubits, as this precession can be exploited to execute quantum operations (see 3.2.2).

The dipole moment associated with the spin of a negatively charged particle is

$$\hat{\vec{\mu}}_{\text{spin}} = g_s \mu_B \frac{\hat{\vec{S}}}{\hbar} \tag{3.8}$$

where for spin $\frac{1}{2}$ systems $g_s = 2$. Electron spin is:

$$\hat{\vec{S}} = \frac{\hbar}{2} \hat{\vec{\sigma}} \tag{3.9}$$

Choosing the B field direction to be on the z-axis such that $\vec{B} = B_0 \vec{e_z}$ the Hamiltonian representing the energy of the system is given as

$$\hat{H} = g_s \mu_B B_0 \frac{\hat{\sigma}_z}{2} \tag{3.10}$$

where $\hat{\sigma}_z$ is the z pauli spin matrix, defined in equation 3.23. Adopting a classical perspective, a spinning mass whose spin axis is misaligned with the "field" (gravity) axis experiences a torque given by

$$\vec{\tau} = \vec{\mu} \times \vec{B} \tag{3.11}$$

where $\vec{\mu} = \gamma \vec{J}$, γ is the gyromagnetic ratio and $\vec{J}$ is the angular momentum. In this context, angular momentum precesses at a frequency $\omega_0 = \gamma B$ since

$$\vec{\tau} = \frac{d\vec{J}}{dt} = \vec{J} \times \vec{\omega} \tag{3.12}$$

Similarly for a quantum mechanical system

$$\vec{\tau} = \frac{d\vec{S}}{dt} \tag{3.13}$$

$$= \vec{\omega_0} \times \vec{S} \tag{3.14}$$

$$= \frac{g_s \mu_B}{\hbar} \vec{S} \times \vec{B_0} \tag{3.15}$$

The electron undergoes precession around the pole at a *Larmor frequency*

$$\omega_0 = \frac{g_s \mu_B B_0}{\hbar} \tag{3.16}$$

The Larmor frequency, which can often be thought of as the qubit frequency, determines the energy gap between the two spin states and is crucial for the control and manipulation of qubit states.

3.2.2 Rabi Driving

In the presence of an in-resonance oscillating orthogonal driving field, a qubit will cycle between its two spin states. This capability to traverse the Bloch sphere is pivotal for realizing quantum circuits and serves as the operational foundation for nearly all condensed matter quantum computing systems. Often the driving field is magnetic, realised via a microwave antenna such as in Chapter 5. In such cases, the total field is

$$\vec{B} = B_0 \hat{z} + B_1(\cos(\omega t)\hat{x} + \sin(\omega t)\hat{y}) \tag{3.17}$$

where the oscillating field is driven at a frequency ω. The Hamiltonian in the driving field subsequently becomes

$$H(t) = \frac{\hbar}{2}\omega_0 \sigma_{\hat{z}} + \frac{\hbar}{2}\omega_1(\cos(\omega t)\sigma_{\hat{x}} + \sin(\omega t)\sigma_{\hat{y}}) \tag{3.18}$$

where $\omega_1 = \gamma B_1$ or *Rabi frequency*, and ω_0 is the Larmor frequency derived in equation 3.16. The derivation of the Rabi formula is widely covered in textbooks [157]; here, I opt to directly present the probability of transitioning between the two spin states:

$$P_{|0\rangle \to |1\rangle}(t) = \frac{\omega_1^2}{\omega_1^2 + \delta\omega^2} \sin^2\left(\frac{\sqrt{\omega_1^2 + \delta\omega^2}}{\hbar} t\right) \tag{3.19}$$

where $\delta\omega = \omega - \omega_0$. Maximum amplitude oscillation is achieved $\omega = \omega_0$. For two-axis control,

essential for realizing arbitrary rotations around the Bloch sphere, a phase term in the driving field is introduced:

$$\vec{B} = B_0\hat{z} + B_1(\cos(\omega t + \phi)\hat{x} + \sin(\omega t + \phi)\hat{y}) \tag{3.20}$$

leading to probabilities

$$P_{x,\,|0\rangle\to|1\rangle}(t) = \frac{\omega_1^2}{\omega_1^2 + \delta\omega^2}\cos^2\left(\frac{\sqrt{\omega_1^2 + \delta\omega^2}}{\hbar}t\right)\cos^2(\phi) \tag{3.21}$$

$$P_{y,\,|0\rangle\to|1\rangle}(t) = \frac{\omega_1^2}{\omega_1^2 + \delta\omega^2}\cos^2\left(\frac{\sqrt{\omega_1^2 + \delta\omega^2}}{\hbar}t\right)\sin^2(\phi) \tag{3.22}$$

Rotation around the two Bloch sphere axes is shown in Fig. 3.3b.

Various methods enable the targeted rotation of electron spins, including electron spin resonance (ESR) [30, 158, 159], electric dipole spin resonance (EDSR) [122, 160, 161], spin-orbit coupling [162–164], AC Stark shifts [165–167], and global field manipulation via a dielectric resonator [7, 8]. These techniques (and many others) achieve the same outcome: the precise alteration of the spin state of a system. Here, I focus on ESR techniques. This method uses a microwave antenna placed proximal to the qubits to generate an AC magnetic field at a specific qubit frequency. Both the phase of the signal and the time-under-resonance dictate the direction and extent of rotation of the spin state around the Bloch sphere. Fig. 3.4 shows a simple gate pulse sequence utilizing ESR. The signal frequency is targeted at the qubit frequency $f_M W = \omega_0$. The spin state of the system is read out using spin-to-charge conversion via Pauli spin blockade. Scanning f_{MW} over a range of frequencies in a double-dot system results in two ESR signature signals, one for the resonances of each dot.

3.2.3 Gate Operations

Combine Rabi driving with precise phase and timing control, and you have the ingredients for single-qubit operations. These operations are composed of 'gates'–basic operations around the Bloch sphere that when combined can realize any arbitrary path. The most fundamental gates are the X, Y, and Z gates, represented as Pauli matrices:

$$X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix},\ Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix},\ Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \tag{3.23}$$

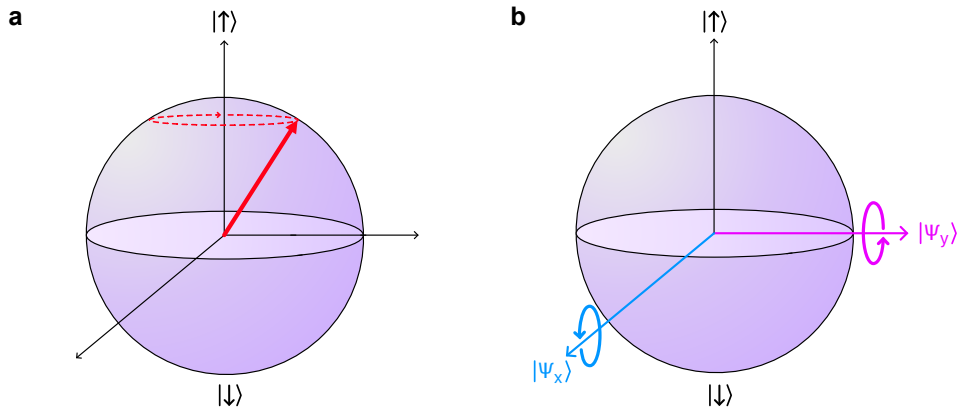

Figure 3.3: **Larmor precession and Rabi driving. a**, Larmor precession around the block sphere. When the qubit state is not pure, it will precess around the pole as indicated. **b**, By changing the phase of the driving field, two-axis rotation for arbitrary single qubit gates is possible. For values of $\phi = 0$, the spin is driven around the x-axis, and for $\phi = \pi/2$, around the y-axis.

To switch from the $|0\rangle$ to $|1\rangle$ state requires precise timing to yield a π-rotation, i.e. $t = \pi/\omega_1$. If the qubit is in a pure spin state, i.e. $|\uparrow\rangle$ or $|\downarrow\rangle$, this is achieved by a X or Z gate. Similarly, many circuits require $\pi/2$ rotations (e.g. $\sqrt{X}$) requiring timing of $t = \pi/2\omega_1$. For example, the Hadamard gate can be represented as a decomposition of X and Y gates such that:

$$H = X\sqrt{Y} \tag{3.24}$$

$$= \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \tag{3.25}$$

Applied to a pure state, the Hadarmard yields an exact superposition:

$$H|0\rangle = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{2}} \end{bmatrix} = \frac{1}{\sqrt{2}}|0\rangle - \frac{1}{\sqrt{2}}|1\rangle \tag{3.26}$$

A simple gate sequence of rotations around the Bloch sphere is shown in Fig. 3.4.

3.2.4 Coherence

Coherence is a measure of how long a qubit retains its quantum state before processes cause it to decohere. Noise within quantum systems fundamentally limits performance, necessitating a comprehensive understanding of its impact on qubits to achieve high circuit depths. In general,

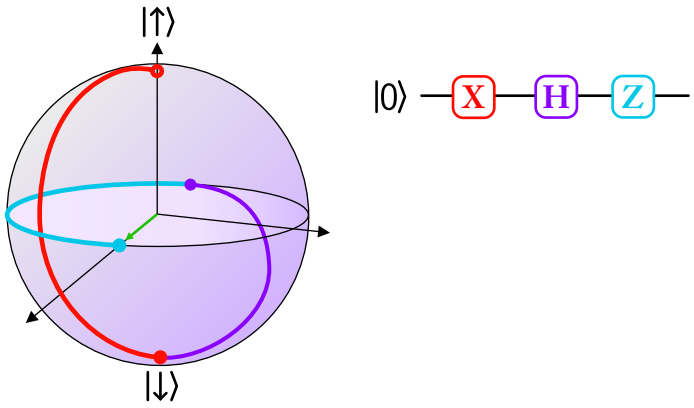

Figure 3.4: **Gate sequence around the Bloch sphere.** Visualisation of a qubit undergoing three gate transformations. The X gate rotates the qubit from its prepared state at the top of the Bloch sphere $|\uparrow\rangle$ to the bottom into a state $|\downarrow\rangle$. The Hadamard gate performs another rotation, this time through both θ and φ to the position shown. Finally the Z gate performs another π rotation about the z-plane to its final destination.

noise processes can be characterized by their impact on certain coherence times, such as T_1 (relaxation) and T_2 processes (decoherence and dephasing). Environmental noise sources like charge noise [168, 169], material impurities causing undesired coupling [170], thermal noise [171, 172], and others contribute to coherence reduction.

T_1 Relaxation: Losing Energy

An electron not in its ground state within a magnetic field relaxes to its ground state spontaneously, or can be relaxed due to noisy fluctuations in the environment; the process is described by the T_1 relaxation time. Relaxation from the exited state to the ground state exhibits an exponential decay:

$$P_{|1\rangle\to|0\rangle}(t) = P_{|1\rangle\to|0\rangle}(0)e^{-t/T_1} \tag{3.27}$$

This exponential decay is shown in Fig. 3.6(a). The T_1 time represents the point at which half of the initial excited spin states have decayed. In SiMOS singlet-triplet systems, T_1 is on the order of hundreds of ms [173].

T_2 Decoherence and Dephasing: Losing Phase Coherence

Beyond just relaxation, a qubit interacting with a noisy environment may pick up a phase shift. These elastic processes cause a loss of qubit coherence. From NMR, T_2 is the pure decoherence time of a qubit due to these energy-conserving environmental interactions [174].

In spin qubit environments, the measured rate of qubit decoherence is much faster than would be expected purely from T_2 alone. Inhomogenous dephasing of the qubit, where its phase becomes poorly synchronised with other systems, acts to shorten the measured T_2 of an ensemble averaged qubit measurement. Inhomogeneities in the local magnetic field contribute to these dephasing processes, stemming from intrinsic variations in the global field or perturbations of local charge sites leading to shifts in the local field. Therefore, a group of T_2-like measurements are used to better characterise the qubit's coherence time.

T_2^* Dephasing An often used metric of qubit performance is the T_2^* coherence time. Simplistically, the fidelity of a qubit is based upon its ability to beat T_2^*, i.e. perform as many operations as possible before significant dephasing occurs. Because T_2^* has no refocusing pulses (see paragraphs below) it acts as a broadband noise probe, sensitive to most noise processes that are likely to impact further qubit operations. Extending T_2^*, therefore, is imperative to achieving higher fidelities. T_2, and consequently T_2^*, are limited to a maximum of twice the T_1 time.

One method of determining T_2^* is a Ramsey interference experiment, shown in Fig. 3.5 (a). A qubit in a pure spin state, for example $|\uparrow\rangle$, is subjected to a $\sqrt{X}$ gate, rotating the spin to the y-axis. The qubit is left to precess about the z-axis for a time t, before a second $\sqrt{X}$ pulse rotates the spin back onto the z-axis. If the driving field frequency is matched to the Larmor frequency, in the rotating frame the qubit remains stationary.[1] If, instead we purposely detune the resonant driving field by frequency $\delta\omega$, then the final state z and x components will oscillate as a function of $\delta\omega$, producinge an exponentially decaying oscillating sine wave known as Ramsey fringes. This is fit using the function:

$$P_{|1\rangle\rightarrow|0\rangle}(t) = P_{|1\rangle\rightarrow|0\rangle}(0)\sin^2\left(\sqrt{\omega_1^2+\delta\omega^2}t\right)e^{-t/T_2^*} + \frac{1}{2} \tag{3.28}$$

This fitting function is similar to equation 3.19. Like an ensemble T_1 measurement, a T_2^* time represents the point at which half of all qubit counts have dephased.

T_2^H Trial-to-trial runs of T_2^* – especially with less ensemble averaging – often exhibit coherence times with significant variation, due to time-dependenct noise processes. By adding a refocusing pulse into the sequence, some of these fluctuations that shorted T_2^* compared to T_2 can be suppressed. This is known as a Hahn echo, or T_2^H, and the full sequence is shown in Fig. 3.5 (b). After the initial $\sqrt{X}$ and t wait time, a X pulse decouples the effects of magnetic noise in the z-axis and spin-spin couplings [175]. The end result is a coherence time longer than the original T_2^* and more

[1] The rotating frame is a reference frame that rotates at the characteristic qubit frequency ω_0.

representative of the intrinsic T_2 time.

T_2^{CPMG} Applying further X pulses similar to the Hahn echo narrows the noise frequency window the qubit is exposed to. By varying wait times t and the number of X pulses this window is adjusted which, when well optimized, extends the decay time further beyond T_2^H. This is known as a Carr-Purcell sequence [176–178], however it is still susceptible to calibration errors resulting in accumulation of under- or over-rotated X pulses.

The Carr-Purcell sequence is extended by inserting Y pulses in place of X pulses which compensate under- or over-rotation on even pulse numbers [179, 180]. T_2^{CPMG} is likely the best estimate for intrinsic T_2. By varying the t wait time and number of pulses, a high resolution a spectroscopic map of the noise the qubit experiences can be generated. This is useful for identifying the behavior of noise within the system, changes in noise as a function of other parameters and to a limited degree the kind of noise affecting the qubit.

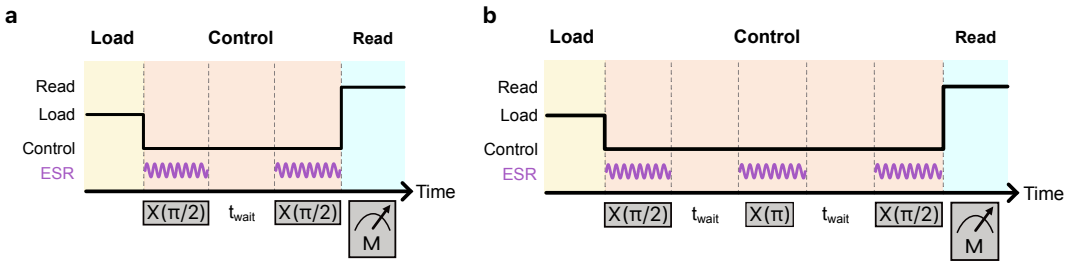

Figure 3.5: **Single qubit coherence pulse sequences. a**, a basic single-qubit pulsing scheme for Rabi oscillations. Here, a gate electrode is pulsed to various voltagelevels for precise state preparation (load), control, and measurement (read). In the control phase, the qubit is rotated using an ESR pulse before waiting for a set period of time (t_{wait}) and rotated identically to analyse the decay in phase over t_{wait}. **b**, compared to Rabi experiments, a Hahn echo incorporate an extra π rotation for dynamical decoupling, decreasing low frequency noise contributions to the decay in signal.

Comparison of the coherence time to the gate time is known as quality (Q) factor. This is a simple equation describing the number of π gate operations possible within the coherence time of a qubit:

$$Q = T_2^{\text{Rabi}}/T_\pi \tag{3.29}$$

Maximizing this number is fundamentally linked to the overall performance of a qubit. T_2^{Rabi} is related to T_2^*, however it is constantly driven on resonance with no free evolution, leading to longer resonance times. Extending T_2^{Rabi}, as well as decreasing gate time through higher ESR power (up to

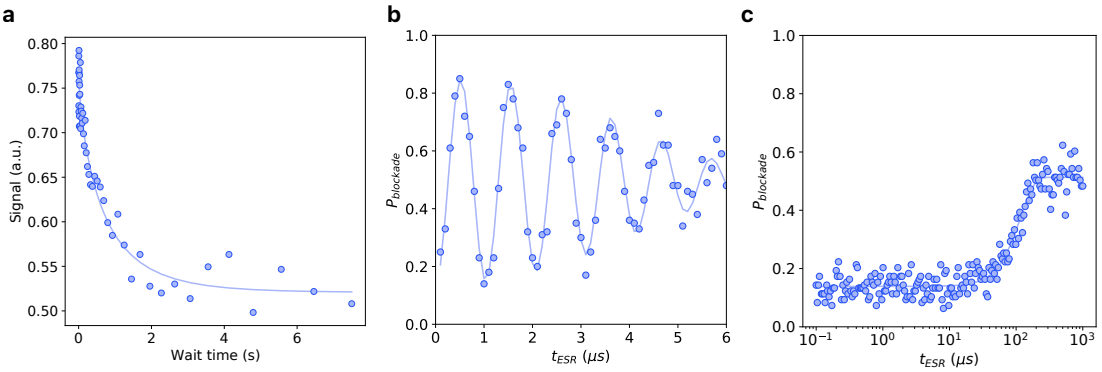

Figure 3.6: T_1, T_2^*, **and** T_2^H **measurements of single qubits.** **a**, fitted T_1 spin relaxation time of a spin qubit. The T_1 time was found to be 690 ms, which is much longer than the typical full measurement and control cycle lasting approximately $1 - 10$ ms. **b**, Rabi oscillation decay to extract T_2^* time. In the first oscillations a near-complete or absent blockade is expected, the lower visibility is attributed to SPAM error in the measurement. These oscillations are present due to pulsing approximately 1 MHz off resonance, thus getting a 1 MHz decaying sine wave to fit to. This technique is optional, and pulsing on-resonance results in data with a similar profile to (c). **c**, a Hahn echo achieves a much longer coherence time (110 μs) versus the T_2^* coherence of 5.6 μs. The dynamical decoupling involved decreases the amount of low frequency noise the qubit 'sees'. Unlike b, here we pulse directly on resonance, avoiding the need for much higher resolution due to the presence of hundreds to thousands of sine waves.

the saturation point or increased noise) are simple mechanisms to increase quality factor. Quality factors exceeding 100 and occasionally 200 have been reported [181–183].

3.3 Systems of Two Qubits

Expanding from a single qubit to a two-qubit system introduces the capability to control a second quantum property: entanglement. This unique quantum-mechanical state allows for the implementation of two-qubit and multi-qubit gates. The following section details fundamentals of the exchange interaction, two-qubit gate operations, and Randomized Benchmarking.

3.3.1 Electron-Electron Interaction

One of the most important behaviors spin qubits are capable of is the ability to interact with one another via *exchange*. This is a short range interaction, similar to the length of the electron wave functions, and is mediated by a gate that controls the tunnel coupling between the two dots. This is known as a symmetric operation, as the gate is (in principle) coupled equally to the two dot gates

either side. Unlike older one-gate-one-dot architectures that rely on detuning [184], the addition of the exchange gate allows for much greater tunability, from zero exchange over several orders of magnitude to exchange rates exceeding the resolution of the classical control electronics [123].

Exchange occurs between pure spin states and mixed spin states. For significantly positive detuning (see Fig. 3.1 (a)) the $S(1,1)$ and $T_0(1,1)$ states are almost degenerate. At zero detuning, the $S(0,2)$ and $S(1,1)$ states hybridize, resulting in an energy splitting between these and the $T_0(1,1)$ state. As the exchange gate increases thee tunnel rate, the ESR spectra of thw two qubits split such as in Fig. 3.7.

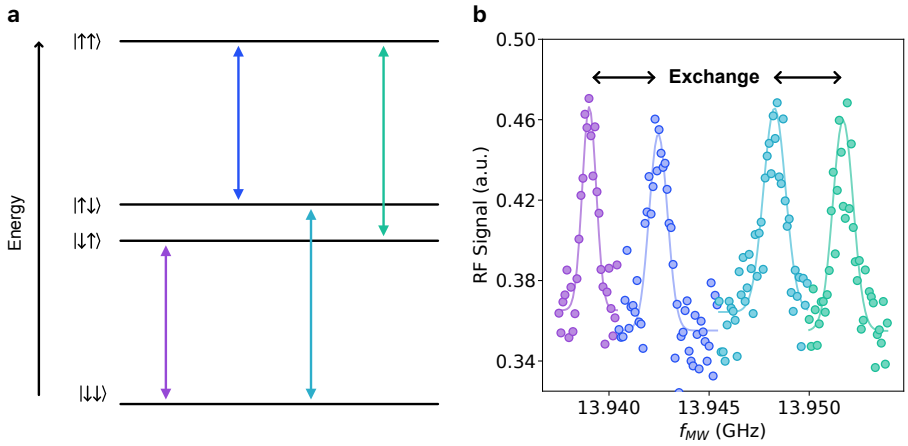

Figure 3.7: **The exchange interaction. a**, Exchange between spin energy levels, corresponding to the peaks in b. **b**, ESR spectrum of two qubits. Due to the high tunnel coupling, exchange opens up between energy levels.

3.3.2 Gate Operations

Many of the two-qubit gates are composed of single qubit gates and a Control-Z (CZ) gate. Here, I cover fundamentals of the CZ gate, as well as CNOT and SWAP gates. The combination of single- and two-qubit gates provides the necessary operations for universal quantum computation.

CZ Family

A CZ gate is a two-qubit quantum gate leveraging the interaction between the two spins. Precise control over the accumulated phase between the $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ states lays the foundation for a more sophisticated gate set.

Two qubits are prepared into a pure $|\downarrow\downarrow\rangle$ state, before a $\sqrt{X}$ rotation on the target qubit spin places it on the equator. A time evolution of the phase occurs during exchange $\phi_{\uparrow\downarrow,(\downarrow\uparrow)}$, contingent

upon the state of the control qubit [185], such that the unitary matrix is:

$$CZ = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix} \tag{3.30}$$

CZ state probabilities as a function of time are shown in detail Fig. 3.9.

Coherence behavior in two-qubit gates closely mirrors that of single-qubit gates. A CZ sequence, akin to a Ramsey measurement but for two qubits, probes a broadband noise spectrum. $T^*_{2,CZ}$ is often similar to T^*_2, due to the similarity in gate sequences. An alternative to extend coherence, similar to T^H_2, is the decoupled-CZ or DCZ gate. A decoupling X gate on both qubits is inserted in the middle of the CZ sequence, which extends coherence by canceling phase errors induced by the Stark shift [186, 187]. Often DCZ gates are chosen over their CZ counterparts, due to this extended coherence as well as relative ease at forming CNOT gates.

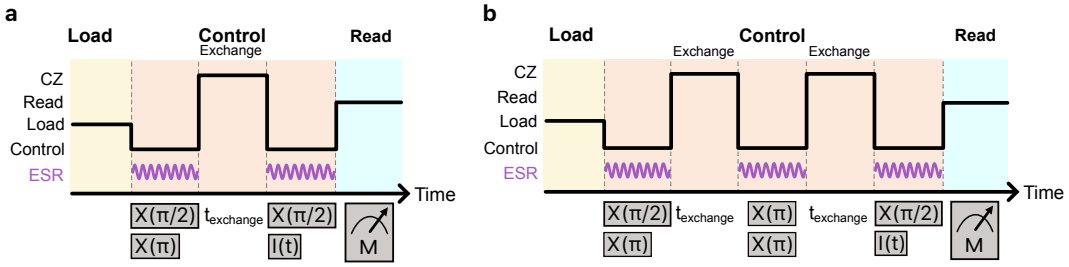

Figure 3.8: **Two-qubit sequences. a**, A simple two-qubit sequence involves the exchange of spin information between the two qubits. $t_{exchange}$ can be calibrated such that the target qubit is rotated by an exact amount desired, dependent on the spin state of the control qubit. This constitutes a control-phase (CZ) gate. **b**, similar to b, by incorporating an echo pulse into the two qubit gate in c, low frequency noise contributions are reduced. This is a dynamically decoupled CZ (DCZ) gate, and can be substituted for CZ gates when desired.

CNOT, SWAP, and Beyond

Realising a CNOT gate involves controlling the exchange time of CZ and DCZ gates such that the accumulated phase $\phi_{\uparrow\downarrow} + \phi_{\downarrow\uparrow} = \pi$. When placing this CZ($\pi$) rotation between two $\pi/2$ (X or Y) rotations of the control qubit, a CNOT gate is formed with unitary matrix:

$$CNOT = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{3.31}$$

Functionally akin to a classical XOR gate, the CNOT gate operates by XOR-ing two qubits, a target and a control, and stores the output in the state of the target qubit. The state of the control qubit, $|0\rangle$ or $|1\rangle$, dictates whether the state of the target qubit remains unchanged or is flipped. However, if the control qubit is initially in a superposition state, the resulting transformation yields a Bell state. Assuming the target qubit is also initially prepared in a $|0\rangle$ state, then the output Bell state becomes:

$$|\psi\rangle = \frac{|00\rangle + |11\rangle}{\sqrt{2}} \tag{3.32}$$

The exact Bell state output is dependent on the prepared state of both the target and control qubits, $|\downarrow\rangle\,|\downarrow\rangle$, $|\downarrow\rangle\,|\uparrow\rangle$, $|\uparrow\rangle\,|\downarrow\rangle$ or $|\uparrow\rangle\,|\uparrow\rangle$. Four Bell states are possible:

$$\left|\Psi^{\pm}\right\rangle = \frac{|00\rangle \pm |11\rangle}{\sqrt{2}} \tag{3.33}$$

$$\left|\Phi^{\pm}\right\rangle = \frac{|01\rangle \pm |10\rangle}{\sqrt{2}} \tag{3.34}$$

Finally, the SWAP gate family is also realised using a combination of CZ(π) and single qubit gates. A SWAP gate directly swaps the computational basis states, and its variations such as $\sqrt{\text{SWAP}}$ and iSWAP are useful for algorithms that employ different levels of coupling between multiple qubits. I direct the reader towards [188, 189] for more details.

3.3.3 Randomized Benchmarking

One of the most effective methods for evaluating the performance of single and two-qubit systems is through randomized benchmarking (RBM), giving a comprehensive measure of gate fidelity [190, 191]. Unlike other evaluation methods, RBM minimizes the impact of state preparation and measurement errors, and averages out coherent errors (such as over- and under-rotations), while simultaneously being scalable to multiple qubits and more efficient compared to other methods like quantum process tomography. While these other aspects are certainly important to the overall performance of a quantum computer, they are less relevant for discussion of noise characterisation

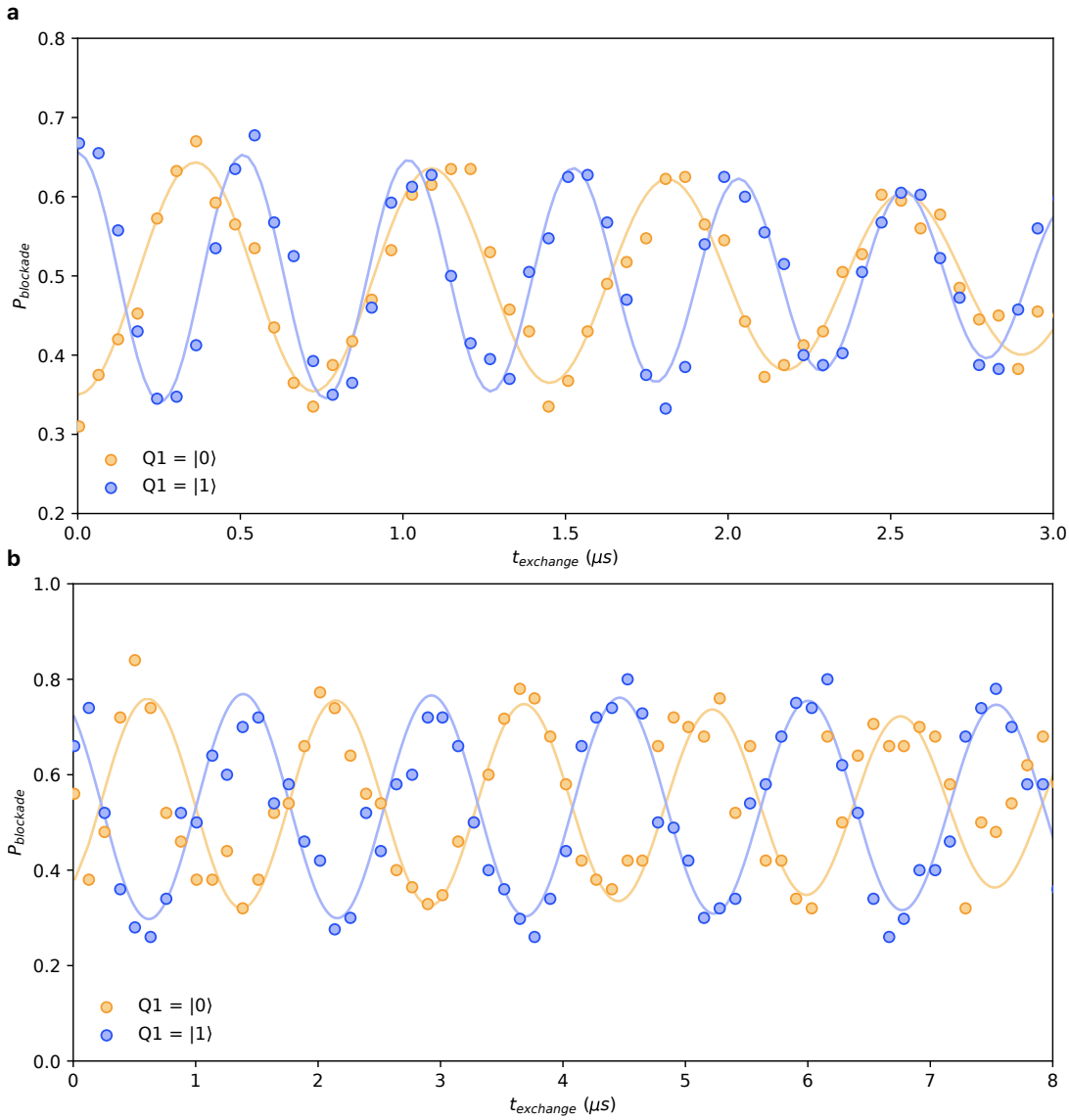

Figure 3.9: **CZ and DCZ oscillations. a**, The spin up probability of a target qubit (Q_2) after a CZ sequence with varying exchange time t_{exchange}. The control qubit (Q_1) is initialised to a spin up (blue) or spin down (yellow) state. **b**, Spin up probability after a DCZ sequence. The control qubit initialisation is in the same as in (a). DCZ operations remove the unconditional z rotations such that calibration of a CZ(π) gate is much simpler.

of qubit gates.

The RBM approach involves executing a series of randomly sampled Clifford gates, followed by a recovery gate and measurement of the final state, as illustrated in Fig. 3.10. Each Clifford gate is unitary, and depending on whether single- or two-qubit RBM is used, comprises only single-qubit gates or a combination of single and two-qubit gates, such as I, X, Y, Z, CZ, and DCZ. With the

addition of each Clifford gate, the probability of the initial and final states being identical decreases due to inherent noise within the system. By analyzing the decrease in this probability (see Fig. 3.10 (a)), a fidelity metric can be derived, which serves as an indicator of the device's performance. The fidelity decay curve is represented as:

$$ae^{-(bx)^c} + d \tag{3.35}$$

where a is bounded by readout fidelity, c represents gate error, and d is approximately 0.5. By interleaving a specific gate between each Clifford sequence, the difference of fidelity serves as an indicator of the performance of that specific gate.

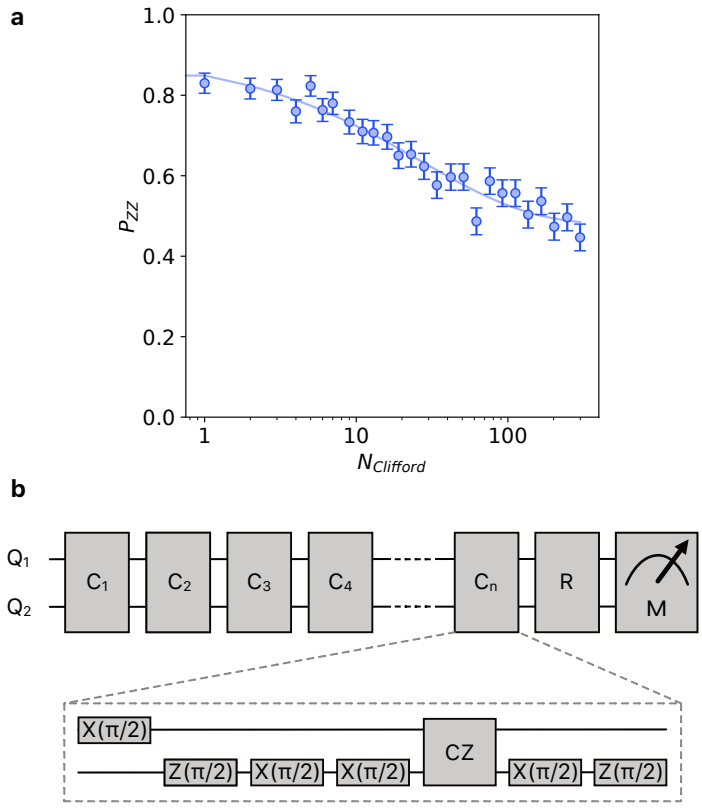

Figure 3.10: **Randomized benchmarking. a** A fitted decay curve of a randomized benchmarking sequence. As more Clifford gates are added, the probability of the qubit returning to its initial state is reduced. P_{zz} indicates the probability of measuring qubits in the $|ZZ\rangle$, otherwise known as the $|00\rangle$ basis state. **b**, A simple schematic of a randomized benchmarking sequence. A set number Clifford gates (C_n) are played in sequence before a final recovery gate (R) and measurement of the state of the system. The recovery gate should in theory reset the qubits back to their initial state. By fitting to the increasing difference between initial and final states over increasing numbers of Clifford gate sequences, a gate fidelity can be extracted. Inset: an example of the constitution of a Clifford gate, made up of single- and two-qubit gates.

3.4 Ten Billion Qubits

The leap to ten billion qubits could be the most formidable engineering challenge of the 21st century. Nearly every aspect of the task requires widening or bypassing a bottleneck, which appear in many different forms. I will not provide a comprehensive overview here, as each sub-field alone constitutes (at the very least) the work of thousands of researchers spanning over decades of work. Instead, I offer a brief, non-exhaustive overview of the obstacles that lie ahead, framed by the central claim of this thesis: quantum and classical systems cannot remain separate if we are to achieve utility-scale quantum computation. Every one of these systems is deeply interconnected, such that even a modest adjustment in one can substantially affect others, and the "best configuration" will certainly involve significant compromises.

3.4.1 The Allure of Boring Devices

Boring is often better. While novel device concepts excite researchers seeking new quantum phenomena, stability and predictability are far more valuable when the goal is to integrate billions of qubits into a coherent system. Within the spin-qubit family alone, there exists a wide variety of possible implementations. Qubits can be realized in different material platforms, ranging from silicon MOS and SiGe heterostructures to carbon nanotubes and donor-based systems. They can be encoded in multiple ways, including Loss–DiVincenzo, exchange-only, or hopping-mode encodings, and may rely on either electron or hole spins. Each of these choices carries far-reaching consequences: material properties influence consistency, performance, and fabrication yield; encoding schemes affect the complexity of control electronics and error-correction requirements; and the decision to use electrons versus holes completely changes the physics of the whole system. Selecting a qubit design is therefore not merely a matter of experimental convenience, but a foundational decision that cascades through every other subsystem in the architecture. A platform that is reproducible, well-characterized, and compatible with existing semiconductor fabrication pipelines may lack the excitement of a novel device, but it dramatically reduces uncertainty in scaling. In short, a boring device built with proven, reproducible techniques and materials may produce useful hardware, while new devices may struggle to achieve any level of utility.

3.4.2 Qubit Layout

One of the most attractive features of spin qubits is their size. Quantum dots nanometers in size offer a greater scaling potential than, for instance, superconducting qubits which are of order mi-

crons in length. But, packing billions of qubits into a dense array is no small feat. Ideally, a ten-billion-qubit system would exist as a $100,000 \times 100,000$ 2D array with exchange control between nearest neighbors. However, as shown in Chapter 5 and given current fabrication constraints, such an arrangement may not be feasible in the near term. Instead, early iterations of utility-scale systems will likely contain small "islands" of qubits, connected via spin-photon links or shuttling channels. Qubit layout has broad consequences: these channels operate with finite speed and fidelity, which affects overall performance, error-correction overhead, and power dissipation. To minimize such costs, qubits should be placed as close together as possible. The same tension arises on the classical side: spreading electronics more widely improves power dissipation and leverages today's fabrication techniques, while tighter integration would demand new methods that could take a decade and billions of dollars to develop. Ultimately, a compromise between quantum and classical systems must be struck.

3.4.3 Thermal Load and Design

Qubits are notoriously fragile. The sole purpose of their surrounding cryogenic infrastructure is to shield them from environmental noise. We're now pretty good at that, regularly and consistently achieving fidelities greater than 99% [192]. The challenge, however, is preserving such isolation as systems scale. This is especially true as classical electronics migrate closer to the qubit plane, a trend motivated by the considerations outlined in Chapter 5. A single qubit and associated integrated electronics, when properly designed, generate a tiny amount of heat, on the order of pico- to nanowatts [193]. When multiplied across a platform containing ten billion qubits, three interrelated problems appear. First, there is a need to dissipate many kilowatts of power within a confined cryogenic environment; second, a qubit temperature below one kelvin must be maintained;[1] and third, thermally isolating qubits from nearby, comparatively warm electronics without introducing high impedance or excess parasitics is necessary but difficult.[2] Much like the issue of fan-out, thermal management is therefore not merely a practical consideration but a fundamental constraint that will shape the architecture of large-scale quantum systems.

[1] And that's being generous! One of the attraction of silicon-based spin qubits is this ability to operate at these "high" temperatures. This is not the case for other qubit modalities, making the cooling problem orders of magnitude more difficult.

[2] It is likely that additional thermal bottlenecks will emerge as scaling progresses, though it remains uncertain which will prove most critical.

3.4.4 Microwaves

Spin-qubit experiments typically rely on AC tones ranging from megahertz to gigahertz, largely serving two distinct purposes. Radio-frequency signals (MHz) are used for fast readout, while microwave tones (GHz) enable both spin manipulation and spin–photon coupling. At small scales this approach is routine, but at the level of billions of qubits, the reliance on microwaves introduces significant challenges, including excessive power dissipation, frequency crowding, and the physical size of microwave hardware. Luckily, mitigating these issues at scale is almost compromise-free as reducing one aspect reduces them all. For example, driving ten billion qubits all at their unique frequencies is farcical, but driving them all at the same frequency [7, 8] simultaneously reduces dissipation, eliminates frequency crowding, and minimizes the number of required microwave components. Similar efficiencies arise from multiplexed readout schemes, which substantially reduce the RF hardware overhead [194]. Nevertheless, key RF elements — such as circulators, resonators, and couplers — remain relatively bulky, a consequence of the microwave wavelength itself. Addressing this size constraint is an active research area [195, 196], with a variety of promising approaches emerging. Importantly, microwave control is not strictly necessary. Certain architectures, such as exchange-only qubits with purely DC-based readout, avoid microwaves altogether, remaining attractive candidates for scaling.

3.4.5 Classical Plane

A system containing ten billion qubits will generate an extraordinary volume of data that must be transmitted, decoded, and acted upon by classical systems in real time. If the classical infrastructure cannot keep pace with the qubits, then executing useful quantum algorithms will remain out of reach. Broadly, this challenge can be separated into two categories: *transmission* and *processing*.

Transmission

Even relatively modest-scale architectures highlight the severity of the data challenge. A 20,000-qubit device is projected to produce data streams exceeding 150 Gb/s [197]. Scaling this to billions of qubits — even under optimistic assumptions involving data compression and encoding — implies data rates approaching hundreds of terabits per second [198], which lies at the edge of current technological capability. Electrical interconnects at such rates would introduce prohibitive levels of heat dissipation and thermal coupling, leaving optical links as the only plausible option. Optical transmission, however, has its own limitations. State-of-the-art wall-plug efficiencies are typically on the order of femtojoules per bit [199], with ongoing progress pushing these limits further [200,

201]. Yet at aggregate rates of hundreds of terabits per second, even femtojoule-scale costs translate into a significant portion of the overall power budget which is particularly problematic when much of this power must be supplied at cryogenic stages. Additionally, while optical fibers provide good thermal insulation, any link bridging cryogenic and room-temperature environments inevitably introduces additional thermal load, increasing the cooling power required to maintain the qubits at operating temperatures.

Processing

Once transmitted to room temperature, the continuous high-bandwidth data stream must be decoded, processed, and acted upon within stringent time constraints. At minimum, the classical system must respond within qubit coherence times, typically on the order of microseconds for conditional operations. Logical operations permit slightly looser timing (milliseconds), but still demand a throughput matched today only by some existing large-scale computing infrastructure. The choice of error-correction protocol will further shape the requirements. For instance, a tailored QLDPC code may offer more efficient logical encoding in certain spin-qubit architectures, but at the cost of significantly greater decoding complexity when compared to a more traditional surface code technique [202]. Efficiently implementing these protocols will require not only advances in algorithms and decoding strategies, but also highly optimized hardware accelerators capable of operating at extreme bandwidths and low latency.[1] Determining the appropriate balance between code design, decoding techniques, and hardware architecture lies well beyond the scope of this thesis, and remains a critical frontier for both computer science and engineering.

The next two chapters detail one tiny part of a world-wide R&D effort to build a utility-scale quantum computer.

[1] The NVIDIA DGX Quantum would be considered today's state-of-the-art for spin qubits.[203]

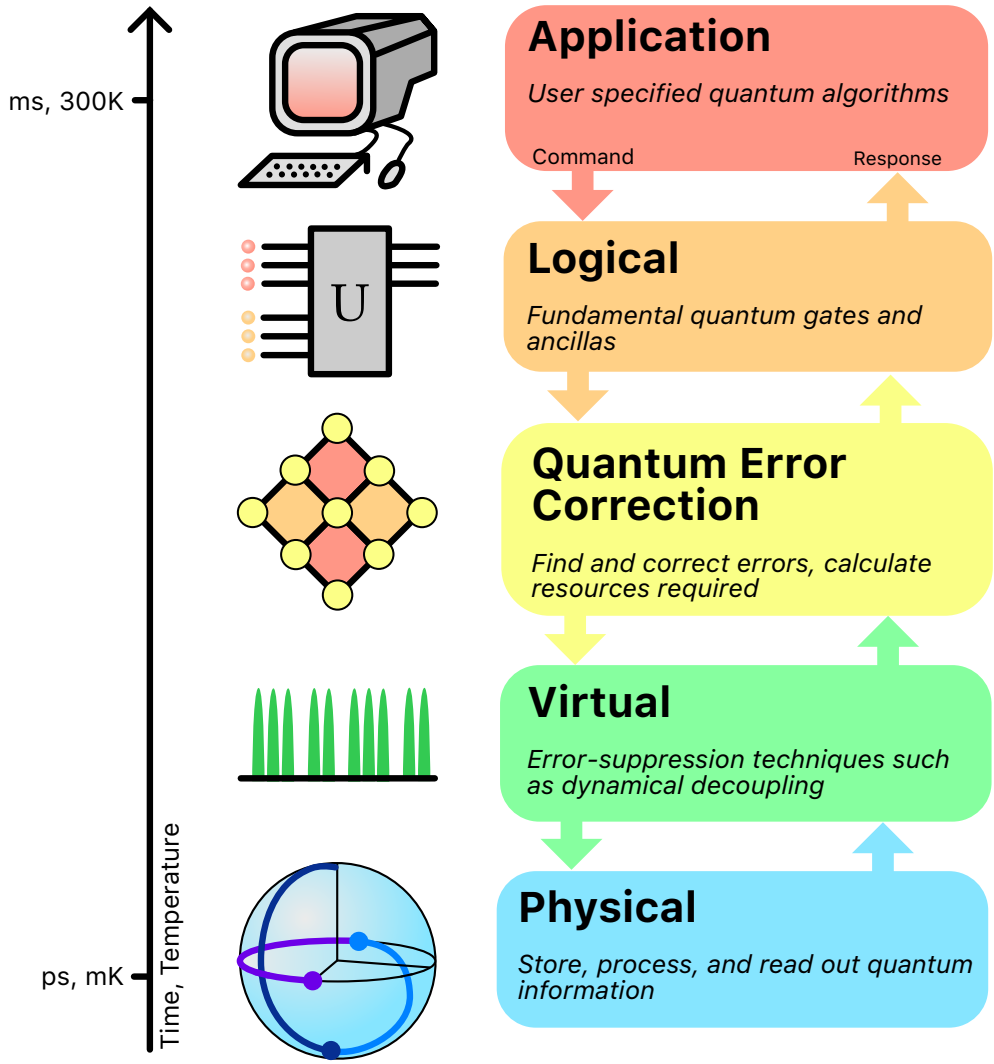

Figure 3.11: **The full stack.** A utility-scale quantum computer requires coordination and mastery of all the layers above. This thesis tackles just one aspect sat firmly within the physical layer.

4

Fast Detection of the Aharonov-Bohm Phase with Gate Reflectometry

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*This chapter is adapted from Bartee et al. *Fast Detection of the Aharonov-Bohm Phase with Gate Reflectometry.* In preparation (2024)

Dispersive gate sensing (DGS) is a scalable, high fidelity means of qubit state readout by locally probing shifts in the quantum capacitance using a single gate electrode. Here, we apply DGS to a (trivial) topological regime, to detect Aharonov-Bohm (AB) and Altshuler-Aronov-Spivak (AAS) oscillations in a gated ring structure created in a 2D electron gas. Comparing DGS to direct transport measurements shows almost identical periodicity and phase for both AB and AAS oscillations. Visibility with an SNR of 1 of the AB phase is achieved over a 60 μs integration time. These results reinforce the viability of measurement-based topological qubits as a platform for realising a scaled-up quantum computer.

4.1 Introduction

Recently it has been theorised that DGS, in addition to Majorana zero mode (MZM) qubit readout, can also provide control via a measurement-only approach [6]. Non-demolitional projective measurements of the topological charge can enable quantum state teleportation, effectively exchanging particles and thereby mimicking braiding [204]. This avoids some of the engineering challenges associated with direct braiding, which proposes a topological "T-junction" for adiabatic exchange of MZMs [205]. Measurement of the joint parity of MZMs is achieved through coupling to quantum dots. Changes to the differential capacitance can be sensed, and thereby shifts in the tunneling rate and MZM system parity can be inferred [206–208]. Validating this measurement-only DGS techniques for MZMs is possible using an appropriate substitute device such as an Aharonov-Bohm (AB) ring. This is an attractive choice, as its magnetic field controllable phase interference serves as an analogue to MZM parity [6].

Past measurements of AB rings are focused solely on transport-based measurement methods, and include investigations of their coupling to quantum point contacts (QPCs) and quantum dots to such systems [209–213]. DGS, meanwhile, is generally limited to quantum dot-based systems where it is presently well understood, with extremely high sensitivity achieved in a number of different architectures [214–216]. In semiconductor spin-based qubit systems—such as the singlet-triplet qubit—DGS readout is achieved via spin-to-charge conversion where the signal arises from a change in occupation (quantum capacitance) of a quantum dot [217]. Macroscopic probing of quantum capacitance via conventional transport techniques is well studied [218, 219], and serves as a foundation for the localised measurements presented here. Compared to conventional DC transport measurements, DGS is a fast and scalable means of performing a phase sensitive measurement, only requiring a single gate. Scalability advantages over traditional RF-reflectometry based readout are realised as source and drain contacts with large ohmic contact regions are no longer required

[216, 220–222].

Here we report on two DGS-enabled AB ring-based devices fabricated from a GaAs heterostructure that detect charge transitions via quantum dot and quantum point contact (QPC) respectively. For the quantum dot, maximum sensitivity is achieved at the electron degeneracy point—at the centre of a Coulomb peak—where there is the greatest change in quantum capacitance. We compare the periodicity and phase of gate reflectometry-based AB measurements to conventional transport techniques. Effective single-shot readout of the AB phase yields a comparable time and fidelity to previous demonstrations of quantum dot dispersive readout [214, 223]. This technique has a broader applicability to probing the magnetoresistance properties of a material, including weak localisation, Schubnikov-de Haas oscillations and quantum Hall effects [224]. It provides a solution to the challenges combining ultra-sensitive, high bandwidth, localised probing and measurement-control of fragile quantum systems.

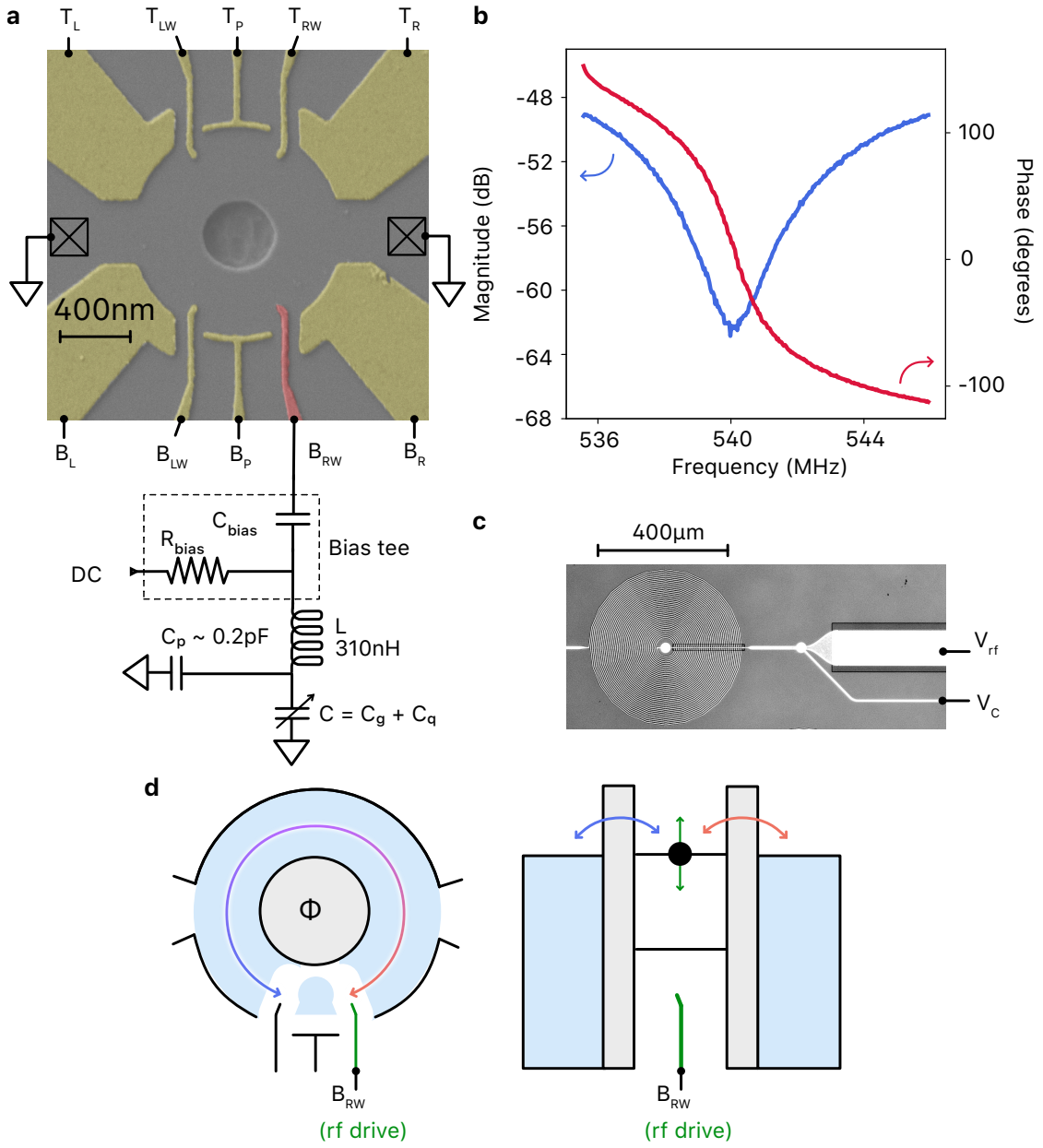

Figure 4.1: **Schematic of the Aharonov-Bohm device a**, False colour micrograph of the device forming an Aharonov-Bohm ring on a GaAs heterostructure. The outer ring boundary is electrostatically defined, and the inner boundary is etched. Crossed boxes indicate the ohmic contacts. The sensing gate BRW is wirebonded to a resonator circuit with an inductor value of L = 310 nH, a parasitic capacitance C_p and gate capacitance C_g. A bias tee is added to allow the application of negative DC voltage to the gate. **b**, Amplitude (blue) and phase (red) reflection coefficients (S12) at zero magnetic field of the resonator. **c**, The resonator consists of a spiral inductor and parallel plate capacitor. The bias tee is also shown allowing for the application of an offset voltage V_C. **d**, Schematic showing electron behavior during DGS. Electron trajectories around the ring gain a phase, and can tunnel on and off the dot when the chemical potential of the ring matches that of the dot.

4.2 Experimental Details

The ring structure used to observe the AB effect is shown in Fig. 4.1 (a). The ring is fabricated on a GaAs/AlGaAs heterostructure (density 1.35×10^{15} m^{-2}, mobility 1.2 million cm^2/Vs), with a 2DEG 91 nm below the surface. The outer ring boundary is electrostatically defined by TiAu gates on the surface of the heterostructure—smaller gate electrodes are integrated into the ring for measurement purposes. Conversely, the inner ring boundary is defined by etching sufficiently deep to remove the 2DEG. By comparing the calculated Fermi wavelength, $\lambda_F = 68$ nm to the width of the ring, we estimate that the device has a maximum of 11 conducting channels. Ohmic contacts, one on each side of the ring, enable four-wire transport measurements and act as capacitively coupled grounds for radio frequency (rf) signals. The device is designed to form a quantum dot, with the sensing gate (red) serving as one of three dot confinement gates. The sensing gate is wire-bonded to an LC resonance circuit, comprising a NbTi spiral inductor (310 nH), with a device-inherent parasitic capacitance (see Fig. 4.1 (c)). A bias tee comprising a parallel-plate capacitor and AuPd resistor, enables the application of DC voltages to the respective sensing gates. All other gates are connected to DC voltage sources only, and gate electrodes are insulated from the surface of the heterostructure stack by 15 nm of aluminium oxide (Al_2O_3), deposited by atomic layer deposition.

The device and resonance circuit are mounted at the mixing chamber of a dilution refrigerator with a base temperature, $T \sim 10$ mK. Reflected (S12) RF signals are amplified at the 4 K stage and analysed directly via a performance network analyser. Our device is designed to allow for simultaneous readout of both DC and DGS signals for direct comparison of the AB effect. In the work reported here, however, signals were not read out simultaneously due to extra interference and noise caused by the excitation and driving of quantum transitions [225].

In order to measure the AB effect, it is necessary to have a variable magnetic field perpendicular to the device plane. The presence of the magnetic field breaks time-reversal symmetry causing an electron to gain a phase ϕ when travelling around the ring in one direction and $-\phi$ in the opposite [226]. The phase difference between the two arms of the ring is determined as $q\Phi/\hbar$ where Φ is the magnetic flux between the two paths. As the magnetic field is slowly changed, the path phases correspondingly evolve between fully in and out of phase. The interference between these two paths produces oscillations in the measured conduction through the ring with a constant period in field. A single oscillation results from a flux change of one flux quantum $\Phi_0 = h/e$. Therefore, the period of the AB oscillations, ΔB, is determined by a change in magnetic flux density equal to one flux quantum within the area of the ring, given by,

$$\Delta B = \frac{\Phi_0}{S} = \frac{2.07 \times 10^{-15}}{\pi r^2} \tag{4.1}$$

where r is the ring radius. This radius is the average between the radii of the inner and outer ring boundaries [227]. Coherent backscattering of electrons within the ring can lead to higher harmonics, in particular resulting in second harmonic AAS oscillations with a single oscillation corresponding to a half-flux quantum change $\Phi_0 = h/2e$. The phase shift—not associated with any part of the loop—has a dependency on the winding number of the electron path [228].

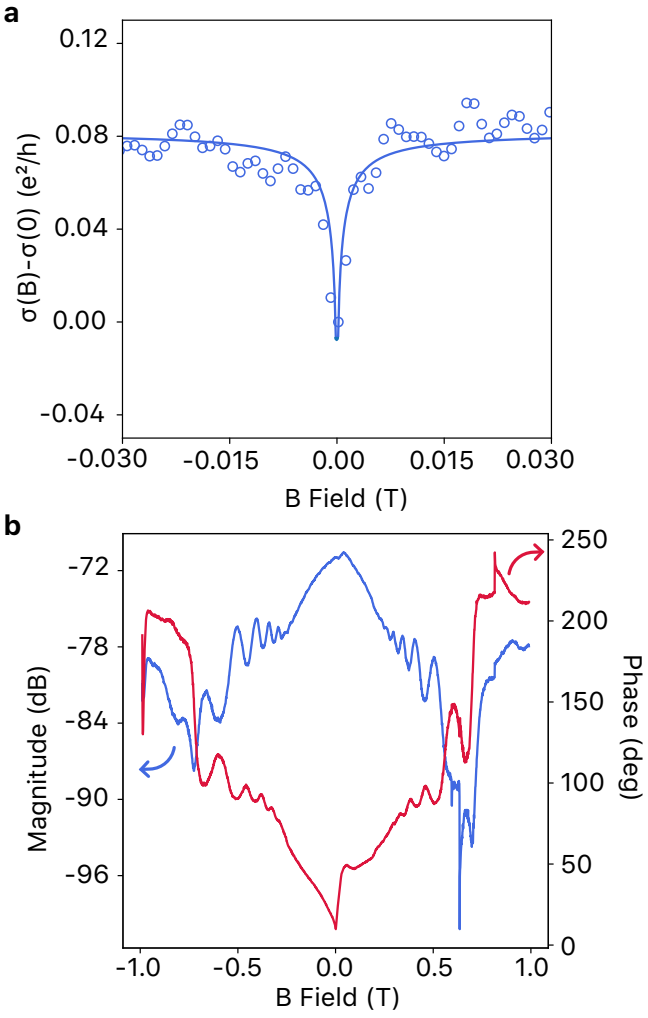

Figure 4.2: **Magnetoconductance through the ring. a**, Magnetoconductance is measured in a Hall bar, in which weak localisation is present. **b**, Measured magnitude and phase signal reflection from the device seen in Fig. 4.1 over the full range of the magnet. Lower field values reveal weak localisation, while higher field values see Schubnikov-de Haas oscillations and weak antilocalisation emerge.

In our device, three gates form a quantum dot within the AB ring to aid DGS. Fig. 4.1 (a) shows gate B_{RW} connected to a resonator, enabling DGS readout via the application of both DC and RF-carrier voltages. Electrons in the 2DEG are depleted underneath the gates and the density of charge around B_{RW} oscillates at the carrier frequency. DGS is sensitive to the quantum capacitance which depends on this density of charge, as capacitance is a ratio of charge that flows in response to an applied voltage. Source and drain ohmics are grounded for DGS measurements so that there is no forward propagation of the electron wave function. Electron trajectories around the ring interfere—the nature of this interference measured at B_{RW} changes with magnetic field, which we see as AB oscillations. A low probability of occupying energy states (destructive interference) cannot induce a charge resulting in a low capacitance value. A high capacitance value at a different magnetic field value due to constructive interference results from a greater response of carriers to the ac voltage. The change in density of states—resulting in a capacitive shift—contains the AB phase as it is related to the probability of occupation which, in turn, depends on the electron wave function interference. The net result is a phase-to-occupation probability conversion measured as an oscillating capacitive response to changes in magnetic field.

4.3 Results

AB oscillations are measured in DC, with the conductance oscillations shown in Fig. 4.3 (a). The magnetic field is ramped at a slow and constant rate, and the conductance found through polling of the device via a four-wire measurement technique. The system is tuned to sit on the side of a coulomb peak, while simultaneously restricting the number of conduction channels through the ring, maximising the amplitude of and sensitivity to AB oscillations. The quantum dot is tuned for optimal RF-measurements, enabling better comparison between the two methods. The first harmonic (h/e) period is found to be 28.0 mT, corresponding to a ring diameter of 307 nm. The physical measured size of the ring was 400 nm, with the difference likely stemming from the sloped etch profile not reaching the 2DEG or Si donor layer at the edges. The Fourier power spectra in Fig. 4.3 (b) show two distinct peaks at 35.7 1/T and 71.4 1/T which correspond to our first and second harmonic ($h/2e$) values respectively. The second harmonic peak in the Fourier power spectrum is consistently smaller than the first harmonic peak, due to increased resistance when travelling twice around the ring [229]. No higher harmonics are routinely observed due to the noise floor of the system.

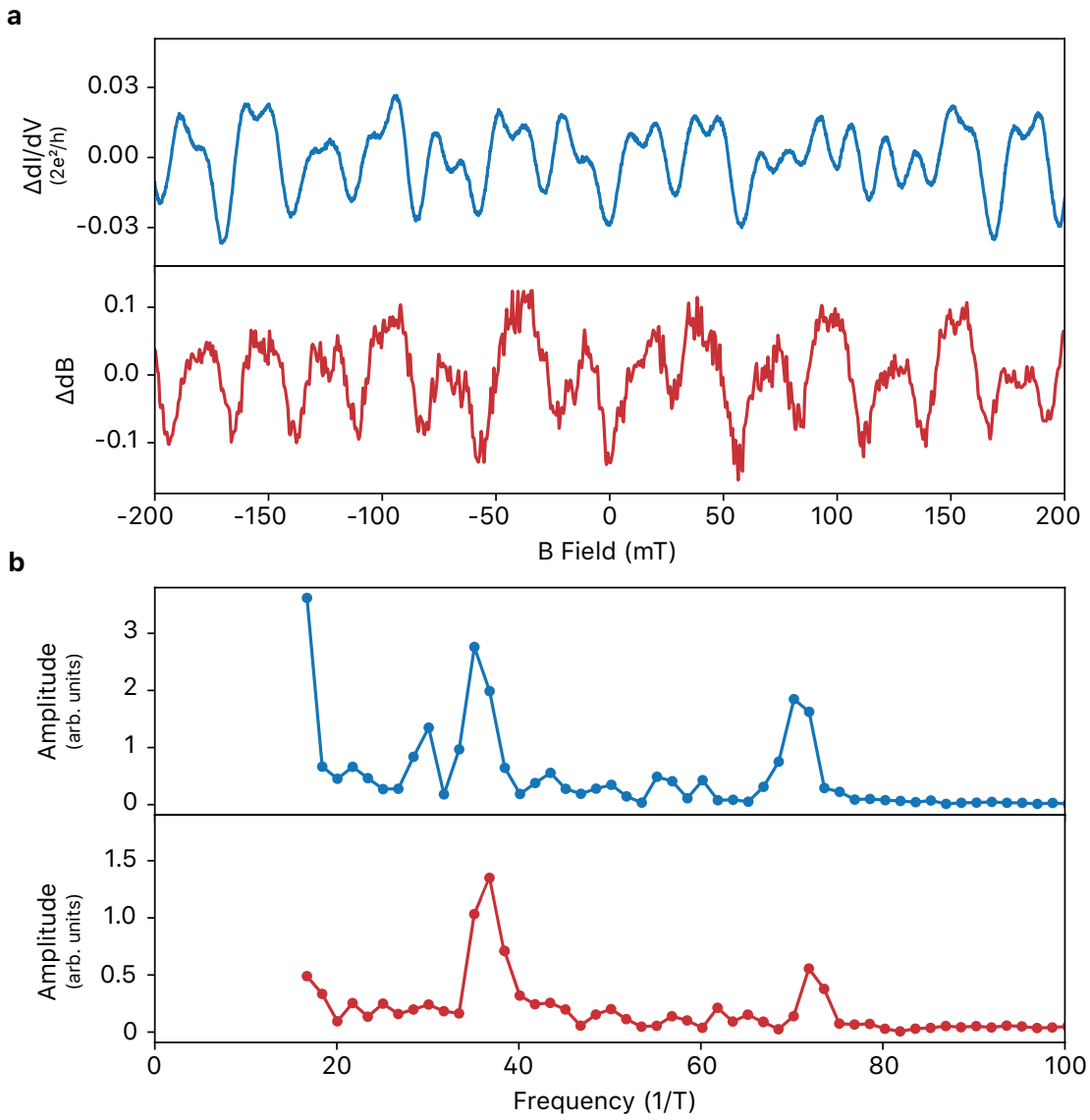

Figure 4.3: **RF and DC-sensed AB oscillations. a**, AB oscillations as a function of magnetic field observed in both a DC transport regime (blue) and dispersive sensing regime (red). Coherent path interference leads to AB oscillations, with other effects at both low and high field values present, such as weak localisation (low) Schubnikov de-Haas oscillations (high) and weak anti-localization (high). Comparing these measurements reveals correlation between the Aharonov-Bohm periods and phases of the two measurement methods. Background information in both DC and RF has been subtracted here. See Fig. 4.6 (c) for the full-field unfiltered measurement. **b**, FFT amplitudes of AB data in (a) demonstrate first and second harmonic interferences, with similar frequency values in both DC and DGS measurements.

Very similar oscillations are observed under DGS of the device. Magnetic field ramp rate and gate tunings are identical to DC counterparts. Comparison of periodicity between conductance and DGS measurements are nearly identical in both devices, well within the margin of error. Using DGS, very similar first and second harmonic periods of 27.8 mT and 13.9 mT are found, as well as an identical relative AB oscillation phase compared to DC measurements. The Fourier power spectrum exhibits many of the same features in the DC version, with consistent peaks at 35.9 1/T and 71.9 1/T. These measurements are performed with no DC bias and no lock-in excitation voltage present. Both DC and DGS measurements shown in Fig. 4.3 have their background subtracted in order to show in better detail the nature of the AB oscillations. The background offsets are approximately -0.6 dI/dV and $+72$ dB respectively, with a full-field unfiltered version of this RF measurement in Fig. 4.6 (c).

To determine the viability of DGS for AB phase readout, we explore the integration time needed to resolve between an AB peak and trough. We seek to prove that the AB phase can be resolved on fast time scales, as it further validates the use of this readout method for MZM-based systems [206, 223]. Similar to previous single-shot measurements of quantum systems, a two-level approach to resolving AB phase is used. This introduces a difficulty, however, as AB oscillations are continuous systems without any discrete energy levels to comparatively measure. Instead, the best two-level approach requires signal data be taken at an AB peak and adjacent trough for maximum sensitivity and most appropriate comparison. Unlike quantum dot systems where rapid switching between states is possible, data must be taken ideally only once at each point in field due to the longer ramping times. This methodology mimics the traditional single-shot measurement of majorana states—the peak and trough of an AB oscillation corresponding to the two-level states of an ideal MZM system.

The SNR of these effective single-shot measurements is determined from the separation and overlap in signal magnitude distributions of the time domain data. Represented as Gaussian distributions, the SNR of the data is calculated by $\frac{\Delta}{2\sigma}$ where Δ is the distance between the peaks and σ is the full width half maximum (FWHM). Noise within the system, which determines the FWHM, largely comprises thermal noise from the cryogenic amplifier, with some low frequency tones present due to the proximity of the pulse tubes.

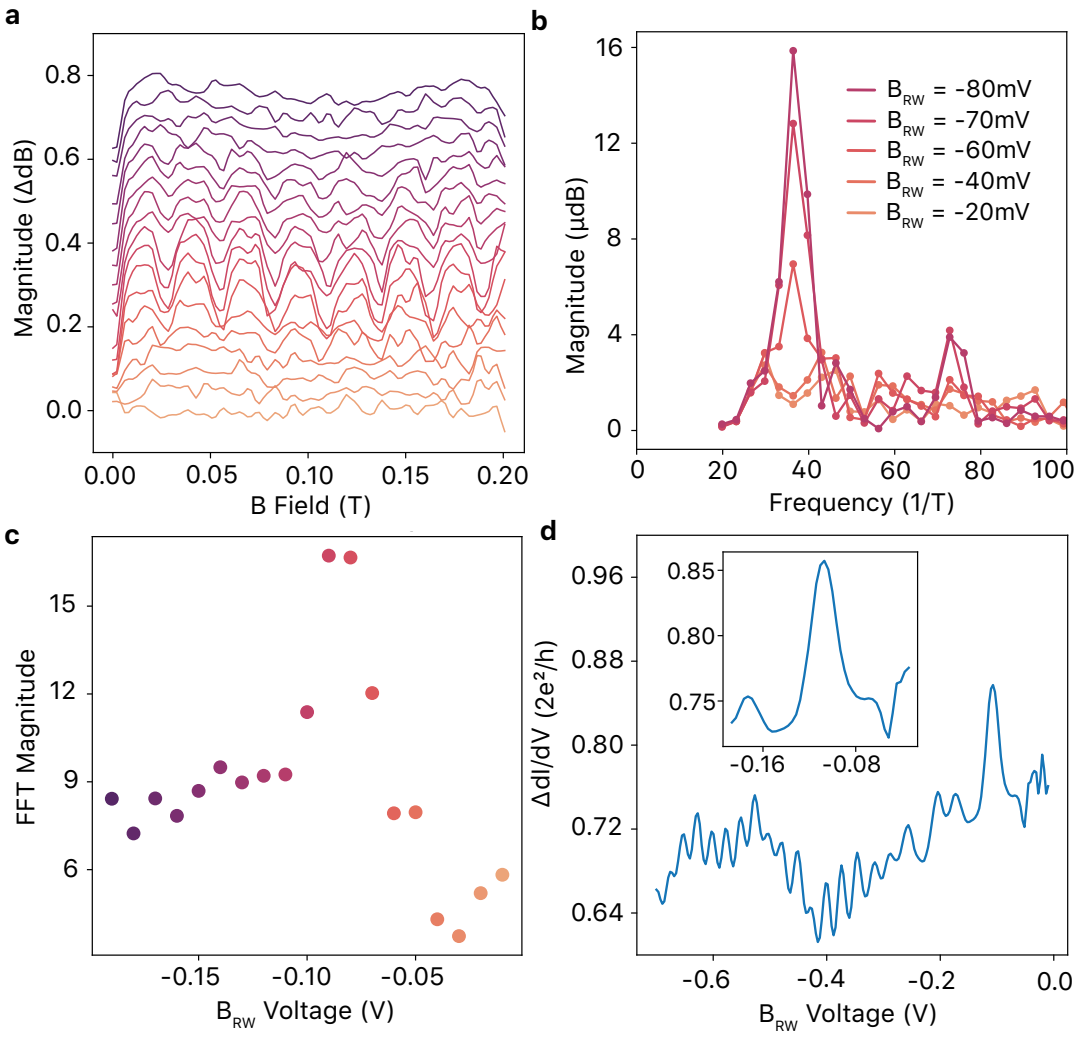

Figure 4.4: **RF sensing window for the AB effect. a**, Unlike DC measurements of this device, the amplitude of Aharonov-Bohm oscillations is extremely sensitive to gate tuning of the sensing gates. As the depletion gates of the device are tuned between open and pinchoff, AB oscillations emerge only in a very specific region of tunings. Traces are offset for clarity. **b**, This behaviour is also evident in the FFT, with the AB and AAS period peaks at 35.9 1/T and 71.9 1/T present for a select few sensing gate configurations. **c**, Shows this in more detail, with the FFT peak at frequency value 35.9 1/T sharply rising and falling over a short range of gate value tunings. **d**, A coulomb peak measured through the ring at the same gate tuning, when both paths are open.

The largest AB oscillations with the minimal background contribution are found at $\sim 700\,\mathrm{mT}$, with the specific peak and trough field values at $703\,\mathrm{mT}$ and $726\,\mathrm{mT}$ respectively. The least amount of background correction is needed for field values $\pm 50\,\mathrm{mT}$, likely reducing error introduced by corrections. Furthermore, the Q-factor at these higher field values is increased substantially, from a value of 140 at zero field to 195 at its height (near $500\,\mathrm{mT}$), increasing sensitivity (see Fig. 4.6 (c)). All gate biases are held at the same values between data sets. A source-drain bias of $0\,\mathrm{mV}$, and a carrier power of $-100\,\mathrm{dBm}$ at the device is found to maximise sensitivity. When factoring in the background envelope, we find we can achieve a readout time of $60\,\mu\mathrm{s}$ with an SNR of 1. These readout times are comparable to those of quantum dots using similar dispersive techniques [214, 223].

AB oscillations are only sensed dispersively in a narrow band of depletion gate tunings (shown in Fig. 4.4). This is in contrast to DC sensing, where the AB effect can be measured over a wide array of gate tuning configurations. As previously stated, this is likely due to the gates requiring enough depletion for non-local charge redistribution, while simultaneously not restricting channels to the point in pinchoff. This experiment does not require the dot be tuned to the single electron regime, and due to the rough edge geometry would prove difficult and may even hinder results. The tuning of the dot itself has a major impact on the sensitivity of the device, likely due to both the coupling of the dot to the ring as well as the overall depletion of the wall gates for large redistribution. Importantly, periodic oscillations are not observed past the pinchoff of any gate in either device, regardless of measurement method.

Several other phenomena are present in the measurements, including weak localization (WL), Shubnikov de-Haas (SdH) oscillations, weak antilocalisation (WAL) and universal conductance fluctuations (UCF). Weak localisation and Shubnikov-de Haas oscillations are particularly evident, as seen in Fig. 4.2. At intermediate field values of $300\,\mathrm{mT}$ to $400\,\mathrm{mT}$, SdH oscillations tend to interfere with AB measurements, exhibiting a similar period and magnitude. This has the effect of potentially skewing the determination of the periodicity when including these regions without adequate filtering. Similar to other experiments, the AB effect can be observed in the ring with the measurement gates tuned to a lower bias, mimicking a continuous ring design [230]. These phenomena are present both in DC and DGS measurements. The phase coherence length l_ϕ was found to be $32\,\mu\mathrm{m}$.

4.4 Discussion

We demonstrate the efficacy of detecting the AB phase on fast time scales using DGS. This serves as an important analog for a topological qubits approach to quantum computing. Importantly, the results found through DGS match those found in DC. We show that we can distinguish between a peak and a trough of an AB oscillation with less than 2% error with only 60 μs of time domain data. This opens up a number of new possibilities for DGS in other topological phases as a fast and robust readout mechanism. As these DGS measurements can be performed without a the need of a source-drain lead, it is not necessary to include the large ohmic contacts that commonly accompany solid state quantum dot measurements. This further improves scalability compared to other RF-based measurement techniques.

Mitigating the problems encountered when forming a QPC or quantum dot against the rough edge geometry of the etched inner ring will likely lead to improved results. While measurements of pure electrostatically-defined rings have demonstrated encouraging outcomes [211], such methods may hinder results here due to the risk of capacitive coupling between the dot and the large metallic island. Coupling of AB rings would bring us one step closer to an MZM-based qubit, better mimicking a hexon-based MZM design [6]. Proven methods of thermal noise reduction can be implemented to reduce readout times further [231, 232]. These approaches, however, are an exciting step in the demonstration of the validity of a measurement-based topological qubit, especially for larger arrays of such devices.

4.5 Supplementary Material

4.5.1 Second Device Performance

The AB effect is measured dispersively on two separate devices, the performance of the second is documented here. This device was also fabricated on a GaAs/AlGaAs heterostructure with the same confinement methods, but with a different gate layout (see Fig. 4.5 (a)). The sensing gate (red) forms a QPC between the gate electrode and the inner etched boundary, and is wirebonded to an identical LC resonance circuit to the first device. Depletion gates either side of the sensing gate help to control and define the QPC along the rough edge geometry of this boundary. This device has a maximum of 6 conducting channels.

Instead of analysing the reflected signal with a performance network analyser, the reflected signal here is demodulated and mixed using a local oscillator at resonant frequency. The subsequent heterodyne signal is passed through a low pass filter and amplified, resulting in a voltage corresponding to changes in the dispersive signal. The resonant frequency of device 1 was found to be $f_0 = 1/\sqrt{LC} = 555$ MHz, with a Q-factor $f_{\text{res}}/\Delta f_{\text{FWHM}}$ of 60 where f_{res} is the resonance of the device. The Q-factor was modulated both by magnetic field value as well as specific device tuning.

Comparison between DC and RF measurements of AB oscillations are shown in Fig. 4.5 (b). The device is tuned to maximise these oscillations in RF, with an identical polling technique used. Using DC measurement techniques, the first harmonic period of this device is found to be 144.7 mT, corresponding to a ring diameter of 135 nm. The Fourier power spectra in Fig. 4.5 (c) show two distinct peaks at 6.91 1/T, 13.82 1/T, which correspond to our first harmonic and second harmonic values respectively. Likewise using DGS, a very similar first harmonic period of 144.5 mT is found. Further, the Fourier power spectrum exhibits many of the same features found in the DC data, with consistent peaks at 6.92 1/T, 13.84 1/T and an interference peak at 3.46 1/T. The first harmonic period is surprising, as the calculated diameter of the ring is 55% smaller than designed at 300 nm. A possible explanation for this is due to the etch profile of the ring; the GaAs etchant likely did not etch all the way to the 2DEG or Si donor region near the outer boundaries.

Effective single-shot readout yielded comparable results. Ideal peak and trough field values (the designated two levels of our system) at 3 mT and 72 mT are used respectively. While weak localisation is found to be present in DGS, its effect is small compared to DC measurements and completely dissipates past 3 mT. A source-drain bias of 5 mV, and a carrier power of -110 dBm at the device is found to maximise sensitivity. When factoring in the background envelope, we find we can achieve a readout time of 55 μs with an SNR of 2. The contrast in readout times of these two devices is likely in part due to the significantly different AB periods. Despite the smaller Q-

factor, the shift in resonance has a larger contribution from the greater change in magnetic field values.

This device requires the depletion gates to be tuned close to pinchoff, as well as the sensing gate tuned to a similar near-pinchoff regime for AB oscillations to be observed dispersively. The QPC overall is found to have a transmission probability of $T_p = G_{QPC}/(2e^2/h) \sim 0.03$ [233]. The near uniform tuning of the depletion gates suggests that while the etched ring is smaller than anticipated, it is still symmetric about the rest of the device.

Similar to the first device, other phenomena are also present in the measurements of this device, including weak localization (WL), Shubnikov de-Haas (SdH) oscillations and weak antilocalisation (WAL).

Unlike previous experiments where oscillations are observed in DC past 4 K [234], oscillations sensed via dispersive means become almost unobservable at T $\sim$ 200 mK and disappear entirely at T $\sim$ 1000 mK. The exact mechanism causing this is unclear, as DGS is sensitive to coulomb oscillations up to 1 K in similar heterostructures [223]. The relatively small capacitive change of AB compared to coulomb oscillations is a likely explanation, as at 1 K the rising noise floor severely decreases sensitivity to these coulomb oscillations and our assumption is AB oscillations are completely washed out by this new noise floor.

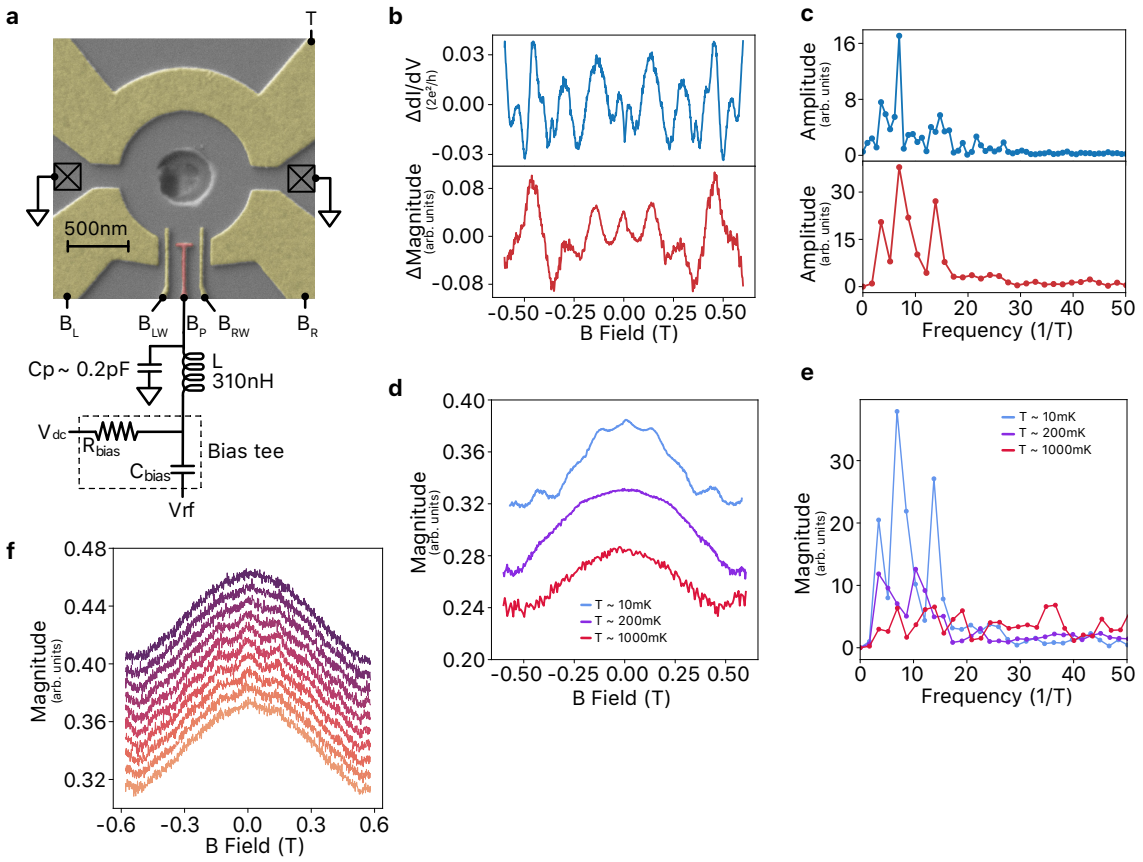

Figure 4.5: **Schematic and major measurements of the second device. a**, False colour micrograph of a second device forming an Aharonov-Bohm ring on a GaAs heterostructure. The outer ring boundary is electrostatically defined, and the inner boundary is etched. Crossed boxes indicate the ohmic contacts. The sensing gate BP is wirebonded to a resonator circuit with an inductor value of L = 310 nH, a parasitic capacitance C_p and gate capacitance C_g. A bias tee is added to allow the application of negative DC voltage to the gate. **b**, AB oscillations as a function of magnetic field observed in both a DC transport regime (blue) and dispersive sensing regime (red). AB oscillation period compared to the first device is much larger due to a smaller etched ring. Comparing these measurements reveals correlation between the Aharonov-Bohm periods of the two measurement methods. **c**, FFT amplitudes of AB data in (b) demonstrate first and second harmonic interferences, with similar frequency values in both DC and DGS measurements. **d**, At higher temperatures, we lose DGS sensitivity of AB oscillations. Traces are offset for clarity. **e**, FFT amplitudes of (d) tell a similar story, with significantly more noise introduced at T = 1 K. **f**, AB oscillations are sensitive to gate tuning of both the sensing and depletion gates, only emerging under a narrow band of tunings. Here the bottom trace has depletion gate tunings of VBLW = VBRW = -59.5 mV, with each subsequent trace an additional 7 mV lower. Traces are offset for clarity.

4.5.2 Further RF Performance

The interaction of the LC resonance circuit with the magnetic field caused the resonance to shift linearly with field. To properly probe the device, the frequency of the transmitted signal was constantly adjusted in conjunction with the magnetic field in order to remain in resonance. Figure 4.6 (a) shows how at higher magnetic fields, the SdH oscillations both laterally shift the resonance as well as change the magnitude of the reflected signal. The data we have does not conclusively show if AB oscillations cause the same effect. Our assumption is that they do, however the relative contribution to resonance or magnitude shifts remains unknown.

The full-field data in Fig. 4.6 (c) shows the full compliment of effects measured in RF. SdH oscillations and WAL have the most impact on the shape of the data, with SdH in particular causing difficulty in the measurement of AB oscillations in certain field regimes. AB oscillations had their greatest magnitude at the peaks and troughs of SdH oscillations around 500-800 mT. Past this point, quantum hall effects tended to interfere with measurements, effectively washing out the AB effect in regions of large magnitude shifts. Phase information yielded many of the same results, however at a generally reduced sensitivity.

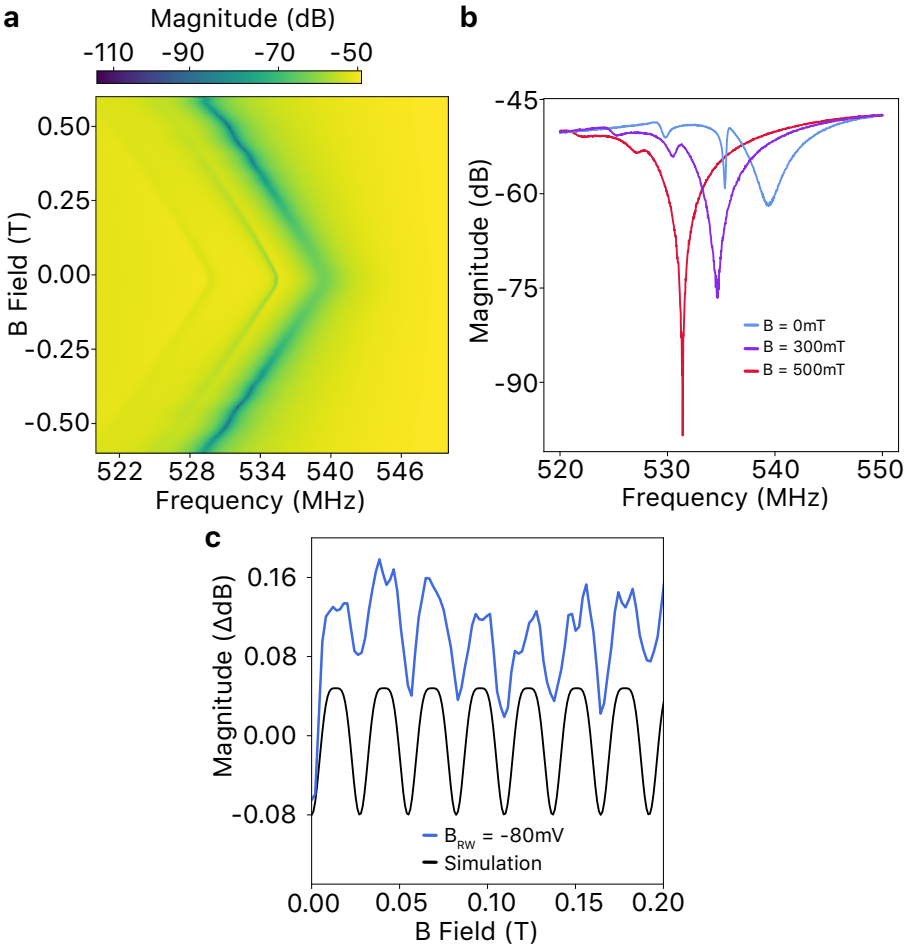

Figure 4.6: **RF sensitivity as a function of magnetic field and AB simulation correlations. a**, The magnetic field is perpendicular to the superconducting spiral inductor of the resonator circuit (see Fig. 4.1 (c)). Changing the magnetic field causes resonant frequency to shift linearly, barring any quantum effects from the device itself. Q-factor also changes with magnetic field, however the nature of these changes is highly dependent on the device performance itself, as well as its tuning. **b**, 1D resonance cut-throughs of (a) at 0 mT, 300 mT and 500 mT. The Q-factor of the resonance grows as the magnetic field is shifted to higher field values. Some contribution is also due to WAL and SdH oscillations present within the data. The exact nature of Q-factor changes with field is dependent on device tuning and geometry. **c**, Comparison between DGS-measured AB phase (reproduced from Fig. 4.4 (a)) and a simulation based on FFT data from Fig. 4.4 (b). The first and second harmonic oscillation phase, period and magnitude of the simulation are in agreement with the measured results. Traces offset for clarity.

4.5.3 Calculation of the Phase Coherence Length

The phase coherence length of the electrons in the ring is calculated by fitting WL using Hikami - Larkin - Nagaoka (HLN) as follows [235]:

$$\Delta\sigma(B) = \sigma(B) - \sigma(0) \tag{4.2}$$

$$= -\frac{e^2}{2\pi^2 h}\left[\Psi\left(\frac{1}{2}+\frac{B_\phi}{B}\right) - \Psi\left(\frac{1}{2}+\frac{B_0}{B}\right)\right] \tag{4.3}$$

Here,

$$B_\phi = \frac{h}{4eD\tau_\phi} \tag{4.4}$$

$$B_0 = \frac{h}{4eD\tau_0} \tag{4.5}$$

$$D = \frac{v_F l_e}{2} \tag{4.6}$$

and Ψ is the Digamma function, $\Delta\sigma(H)$ is the change in magneto-conductivity, B is the magnetic field, v_F is the Fermi velocity, and l_e is the elastic scattering length [236] [237]. From this, l_ϕ can be extracted.

The value of l_ϕ was extracted from weak localisation data of a Hall device on the same chip the AB device was measured, and found to be 32 μm. Weak localisation in the AB rings is also present, however the width of the ring channels falls within the 1D regime and introduces further complexities with the interaction of the AB phase [238] [239].

4.6 Acknowledgements

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5

Spin Qubits with Scalable milli-kelvin CMOS Control

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A key virtue of spin qubits is their sub-micron footprint, enabling a single silicon chip to host the millions of qubits required to execute useful quantum algorithms with error correction [13, 240, 241]. With each physical qubit needing multiple control lines however, a fundamental barrier to scale is the extreme density of connections that bridge quantum devices to their external control and readout hardware [12, 194, 242]. A promising solution is to co-locate the control system proximal to the qubit platform at milli-kelvin temperatures, wired-up via miniaturized interconnects [1–4]. Even so, heat and crosstalk from closely integrated control have potential to degrade qubit performance, particularly for two-qubit entangling gates based on exchange coupling that are sensitive to electrical noise [243, 244]. Here, we benchmark silicon MOS-style electron spin qubits controlled via heterogeneously-integrated cryo-CMOS circuits with a low enough power density to enable scale-up. Demonstrating that cryo-CMOS can efficiently enable universal logic operations for spin qubits, we go on to show that mill-kelvin control has little impact on the performance of single- and two-qubit gates. Given the complexity of our milli-kelvin CMOS platform, with some 100-thousand transistors, these results open the prospect of scalable control based on the tight packaging of semiconductor qubits with a 'chiplet style' control architecture.

5.1 Introduction

Utility scale quantum computing will likely require millions of physical qubits, operated via auxiliary classical systems that generate more than a trillion control signals per second [245, 246]. In realizing such a vast and complex platform, silicon qubits present advantages with their small footprint [247], long coherence times [173], and inherent compatibility with very large scale integrated (VLSI) control circuits. While the potential for integrated control has been a key motivator for the progress in silicon-based qubits over the last two decades, to-date this aspect has remained largely undeveloped.

Despite the advantages of integrated control [12, 194], a serious concern arises from the heat and crosstalk generated by modern CMOS circuits. In relation to heat, this problem is eased by recent work showing that spin qubits continue to function at elevated temperatures [248–250]. Nevertheless, two-qubit entangling gates remain exquisitely sensitive to electrical noise [243, 244], arising for instance from volt-scale, sub-nanosecond switching of proximal CMOS transistors. One means of partially mitigating these adverse effects is to separate the control system to 4 kelvin, connecting to milli-kelvin qubits via long cables [2, 251]. Unfortunately, cable connectivity poses an additional barrier to scaling up the control interface [194] given the extreme density of interconnects required to operate even modest numbers of qubits.

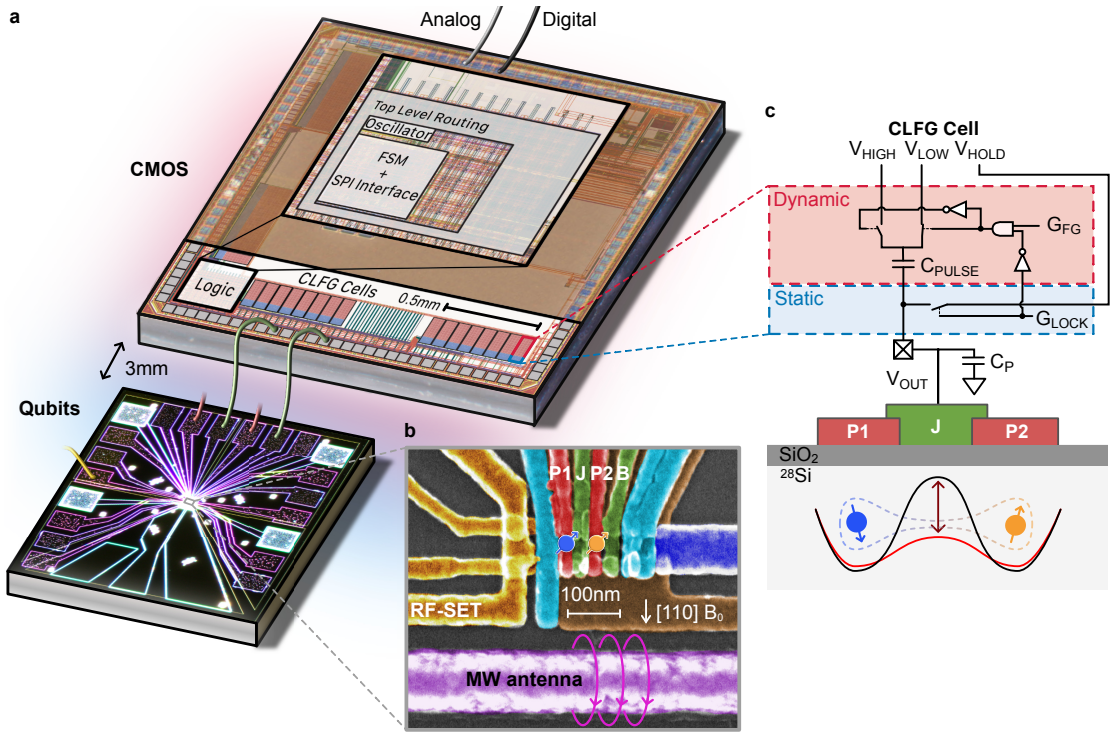

Figure 5.1: **Device and basic CMOS operation.** **a**, The cryo-CMOS and the qubit chip are mounted on the same board at mK temperatures and wirebonded together. All other control systems are at room temperature. **b**, cryo-CMOS features, wirebonding connections to the silicon device, and an SEM image of a nominally identical silicon device. There are 32 CLFG cells on-chip, one of which is connected to gate J that controls the coupling between the two quantum dots. The other cell is connected to gate B, which acts as an additional barrier gate. All other fast-pulse gates ($P1$, $P2$, SET) and DC barrier gates are connected solely to room-temperature electronics. **c**, schematic of a charge-locking-fast-gating (CLFG) cell and its electrical connection to gate J of the silicon device. Pulsing on this gate acts to modulate the tunnel coupling between the two spin qubits, an essential operation for single- and two-qubit control.

Here, we demonstrate the control of MOS-style silicon spin qubits using a heterogeneously-integrated cryo-CMOS chip operating at milli-kelvin temperatures, as shown in Fig. 5.1 (a). Heterogeneous, 'chiplet style' integration, as apposed to monolithic circuits, decouples the hot and noisy control system from sensitive qubits and retains the potential for dense, lithographically-defined chip-to-chip interconnects needed to manage the wiring challenge inherent to spin qubits. We demonstrate this chiplet architecture supports a control scheme that leverages a global resonance field to enable complete universal control of spin qubits using the baseband pulses that can be generated efficiently with proximal, low-power cryo-CMOS.

The details of the CMOS control chip have been reported previously with an early conceptual demonstration using GaAs quantum dot structures [1]. The effect of milli-kelvin CMOS on qubit performance however, has remained an open question until the present work. Naively, since the spin degree of freedom is somewhat decoupled from electrical noise, integrated CMOS is expected to have only a minor impact on single qubit operations. In contrast, coupling spins via Heisenberg exchange creates the most sensitive probe of voltage noise known [243, 244] since the exchange energy can depend exponentially on gate voltage. Countering this intuition, we show that even for noise-sensitive two-qubit gates, our chiplet architecture, comprising some 100-thousand transistors, does not lead to a measurable reduction in coherence time.

5.2 Experimental Platform

An electron micrograph of a silicon-metal-oxide-semiconductor (SiMOS) qubit device is shown in Fig. 5.1 (b). The device is fabricated on an isotopically purified ^{28}Si epilayer with residual ^{29}Si concentration of 800 ppm [252], and SiO_2 isolating layer with metal gates patterned in aluminium. Quantum dots hosting single spin qubits are formed under the plunger gates ($P1, P2$) at the Si/SiO_2 interface, and an exchange gate (J) modulates the tunnel coupling between the two dots, essential for two-qubit operations. A radio-frequency single-electron transistor (RF-SET) [253] detects the charge state of the quantum dots on microsecond timescales by leveraging an off-chip LC resonator operating near 400 MHz [254], and a proximal microwave (MW) antenna generates an oscillating magnetic field for spin resonance control (see Fig. 5.1 (b)).

The exchange gate J and a boundary gate B are both wire-bonded to the cryo-CMOS control chip [1] which is implemented in 28 nm fully depleted silicon-on-insulator technology (FDSOI). The chip contains a serial peripheral interface (SPI) to handle digital input instructions and a finite state machine (FSM) for on-chip digital logic. The FSM configures 32 analog 'charge-lock fast-gate' (CLFG) circuit blocks, each of which can be used to control a gate electrode on the quantum device

(see Fig. 5.1 (c)). In this configuration, the charge is periodically stored and shuffled between small capacitors, leveraging the low leakage of transistors at cryogenic temperatures that maintain the potential during quantum operations. The cryo-CMOS chip also incorporates a ring oscillator and configurable register designed as a programmable internal trigger (see Extended Data Fig. 5.7 (a) for oscillator schematics). Here, for convenience, we opt for external triggering.

The core functionality of a CLFG cell is to lock a static voltage bias and enable a fast pulse between two voltage levels, as outlined in Fig. 5.1 (c). For instance, targeting gate J, the CLFG cell is programmed to first bring the gate to a potential V_{OUT}, equal to the potential V_{HOLD} of an external source. Opening the switch G_{LOCK} under control of the FSM then 'charge locks' this potential on the gate capacitor. Even though this floating capacitor is now galvanically disconnected from the source, a pulse can be induced by toggling the potential on the upper-plate of this capacitance between V_{HIGH} and V_{LOW}, as shown in Fig. 5.1 (c). This toggling is produced autonomously by the programmed on-chip FSM, leading to a modified output V_{OUT} by: $\Delta V_{\mathrm{PULSE}} = (C_{\mathrm{PULSE}}/C_{\mathrm{P}} + C_{\mathrm{PULSE}}) \cdot (V_{\mathrm{HIGH}} - V_{\mathrm{LOW}})$, where C_{P} is the parasitic capacitance. This mechanism has previously been shown to produce pulse amplitudes of 100 mV at a power of ~ 20 nW/MHz [1]. Below, we demonstrate how this architecture can be used to efficiently control spin qubits.

5.3 Experimental Results and Demonstrations

Turning to evaluate single qubit gates, we first establish a baseline using all room-temperature (RT) electronics for control. Following the usual protocol for two-spin manipulation [240, 255, 256], the singlet state is first prepared in the (1,3) charge configuration using pulses applied to detuning gates $P1$ and $P2$, [with (n,m) labeling the number of electrons in each dot under $P1$ and $P2$ respectively]. A pulse applied to the J-gate, connected to V_{HOLD}, then increases the barrier, separating the two electrons into each dot where they are independently addressed using the MW antenna via their unique resonance frequency (f_{ESR} = 13.9 GHz for a field B_0 = 0.5 T). Free-induction decay (FID) of the target spin is produced by applying MW power to the on-chip ESR line. Finally, a second pulse of the J-gate returns the spins to the readout configuration where Pauli spin blockade (PSB) enables spin-to-charge conversion [108, 109] and measurement via the RF-SET. The shot-averaged readout signal as a function of MW power and frequency is shown in Fig. 5.2 (a). Beyond FID, we further establish our RT baseline by performing pulse sequences implementing Hahn echo (to measure coherence time T_2, see Extended Data Fig. 5.8) and randomized benchmarking (to measure qubit control fidelity) [190, 191].

In this single-qubit measurement, the function of the J-gate pulse is to separate the two-spin

system for controlled rotation via spin resonance. As such, electrical noise, coupled via the J-gate or other means is unlikely to impact qubit fidelity in the limit that the pulse amplitude and duration are sufficiently large to fully separate the spins. Even so, we now evaluate the impact of cryo-CMOS control on single qubit performance by performing the same protocol outlined above, but now with charge-locking applied to the J-gate and the pulse produced using a CLFG cell under control of the FSM. Again we generate FID data and quantitatively compare between CMOS and RT control using randomized benchmarking protocols, as shown in Fig. 5.2 (b). A slight degradation in qubit fidelity is observed (0.07%), likely due to unmitigated heat from the CMOS. We discuss heating in detail below.

Although electrical noise on the J-gate does not directly couple to single spins, heat and drift in gate potential over longer timescales can impact qubit performance. Gate noise can also dc-Stark shift the qubit frequency in certain regimes (discussed further below). To further investigate these mechanisms we extract the time-ensemble average coherence time T_2^* for each qubit, repeatedly measured as each circuit block of the CMOS chip is powered-up. Comparing this data in Fig. 5.2 (c) again shows a small impact with respect to our RT baseline, correlating with a slight rise in the base temperature of the refrigerator (see figure caption for details).

A drawback of the control scheme outlined above is its reliance on qubit-specific microwave pulses, which, despite cryo-CMOS gate control, still requires additional RT pulse generators (and cables) for each qubit. We next demonstrate an alternate control approach that leverages a continuous wave (CW) global microwave field, sourced from RT but common to all qubits [247, 257]. Key to this scheme is the ability to tune the spin resonance frequency of a qubit using a gate voltage [258]. This dc Stark shift enables a gate pulse to bring a qubit into resonance with the global field for a controlled amount of time to produce a rotation in the qubit state vector. With a single microwave tone from RT, cryo-CMOS produces the 'baseband' gate pulses that independently bring each qubit into and out of resonance with the global field.

The global-MW scheme requires a calibration of the unique dc-Stark shift produced by the J-gate on say, qubit Q_2, as shown in Fig. 5.3 (a). The sizable shift (~ 1 MHz/10 mV) is well-matched to the voltage pulses that can be efficiently generated with proximal low-power CMOS. Here, the spins are initialized in the (T^-) ground state via off-resonance relaxation, with the J-gate pulse producing the time-controlled Stark shift. Repeating this sequence as a function of pulse length yields the coherent oscillations shown in Fig. 5.3 (c). For this measurement, the width of the pulse is set by the timing of the trigger fed to the CMOS from RT. Conceptually, this reliance on RT triggering may appear to be a limitation of our CMOS circuits, however, we note that fine time resolution is only needed to map out coherent oscillations. In contrast, once calibrated, logic gates

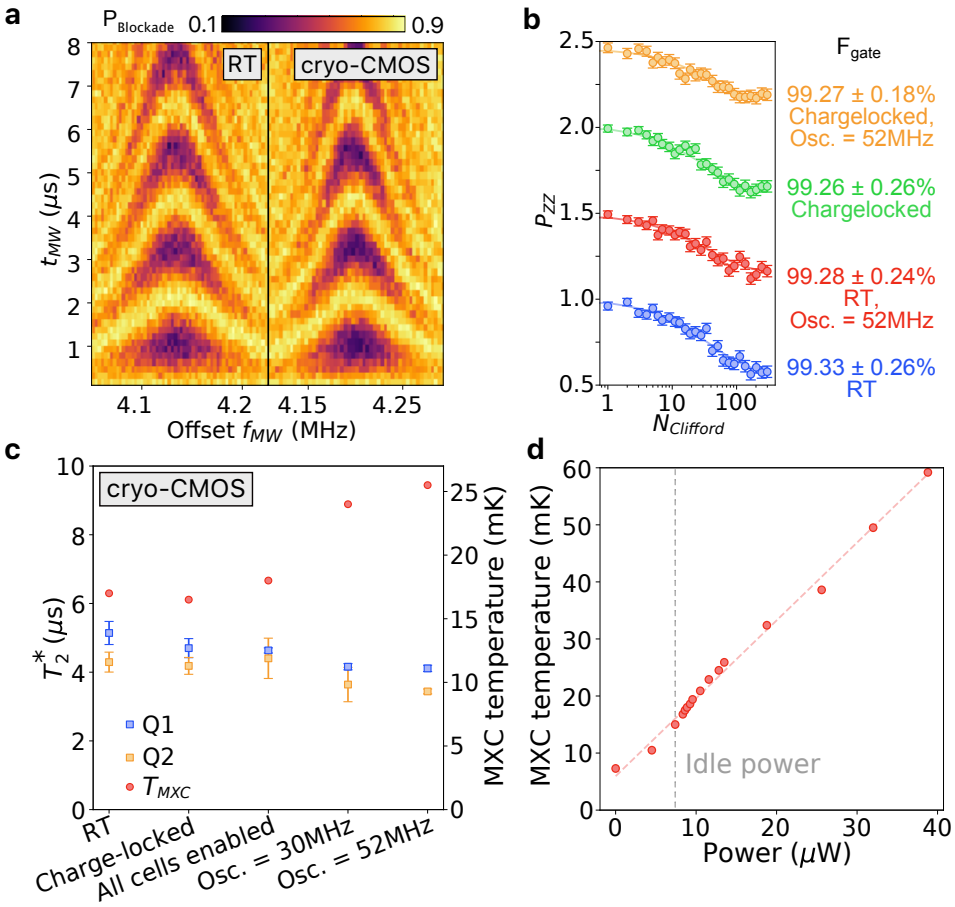

Figure 5.2: **Benchmarking single qubit cryo-CMOS performance**. **a**, Single-qubit Rabi oscillations as a function of microwave frequency f_{MW} and pulse time t_{MW}, performed with RT control. **b**, Single qubit randomized benchmarking under various cryo-CMOS conditions. Traces are offset for clarity. **c**, Single qubit T_2^* coherence time as a function of select cryo-CMOS parameters. Unless otherwise indicated, all data taken here uses cryo-CMOS control. **d**, Correlation of the reported mixing chamber temperature with cryo-CMOS power draw.

require a fixed time pulse, for instance, 1 μs to produce a $\pi/2$ rotation. As such, these fixed time pulses are straightforward to implement with our CMOS architecture.

Lastly we turn to evaluate two-qubit logic gates, which provide the most stringent test for crosstalk or electrical noise stemming from proximal milli-kelvin CMOS control. Here, the target qubit is rotated about the Z-axis depending on the state of the control qubit, with the gate-tunable exchange interaction modulating the coupling between the two electrons [240, 255]. As a baseline we first perform a decoupled controlled phase gate (DCZ) using all RT instrumentation. The DCZ gate incorporates a spin-echo sequence with coherent rotation about the Z-axis of angle $\phi = J(\epsilon)t_{ex}\hbar$, enabled by turning-on exchange for a controlled time with J-gate pulse of duration t_{ex} (see Extended Data Fig. 5.6 (d)). The resulting readout probability with J-gate pulse width is shown in Fig. 5.4 (a). The DCZ gate is sensitive to high-frequency electrical noise arising either directly from exchange-gate voltage fluctuations or, indirectly, from noise in the (gradient) magnetic field or variation in g-factors from gate-induced movement in position of the electron wavefunction.

Comparing now cryo-CMOS control to our RT baseline, we observe that the coherent exchange oscillations shows similar behaviour, as shown in Fig. 5.4 (b). These results immediately confirm the utility of proximal milli-kelvin CMOS for controlling two-qubit logic gates. Close inspection perhaps suggests a suppression in visibility for the CMOS data, however this can be explained by the available resolution during readout and preparation phase, as opposed to during control.

As a noise diagnostic tool, it is also worth noting that the DCZ gate is somewhat limited since the spin-echo sequence decouples the spin dynamics from low frequency noise. Removing the echo pulses then opens the bandwidth to now include all of the low frequency components down to quasi-dc, offering a better measure of the total aggregate noise inherent in the system. A comparison of RT control with CMOS is made in FID data shown in Fig. 5.4 (c), now without spin-echo. These datasets constitute a measure of the ensemble average coherence time associated with the exchange gate, $T^*_{2,CZ}$. Lastly, using this parameter as a wideband measure of noise, Fig. 5.4 (d) compares $T^*_{2,CZ}$ for RT control, cryo-CMOS with a single charge-locked cell, all cells locked (mirroring J-gate pulses), and as a function of CMOS oscillator frequency. A slight reduction in $T^*_{2,CZ}$ ($\sim$ 20%) is observed at the highest clock frequencies, which, given the slight corresponding increase in refrigerator temperature, likely stems from parasitic heating.

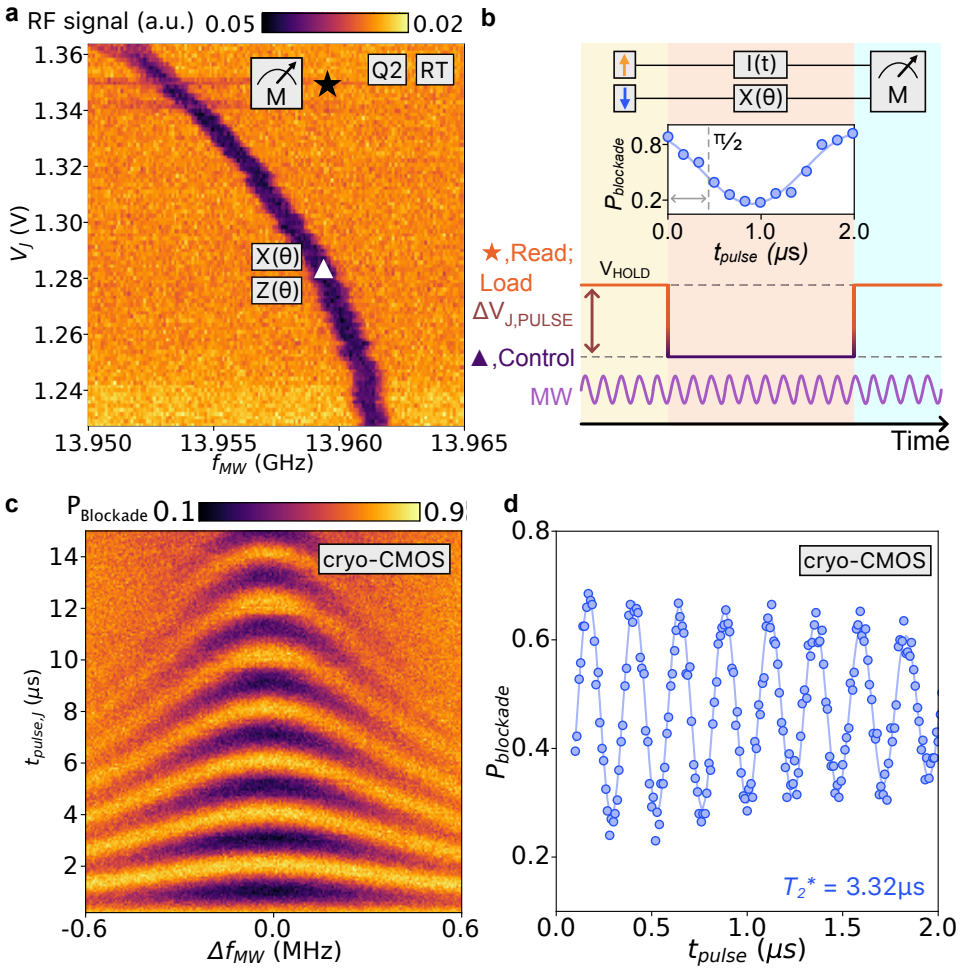

Figure 5.3: **Single qubit gates with cryo-CMOS. a**, ESR spectra as a function of microwave frequency and J gate voltage. Q_2 exhibits a significant Stark shift, which allows for on-resonance single qubit operations (X, Z; ▲), and off-resonance loading and measurement (M; ⋆). **b**, Schematic of the pulsing sequence when using effective global control. Qubit rotations are determined by J pulse time, with the MW tone fixed to the maximum t_{pulse} time, extending into load and read stages. **c**, Rabi chevron of Q_2 and **d**, Ramsey coherence time, using global control and cryo-CMOS pulsing at $B_0 = 0.5$ T. Cryo-CMOS pulsing is enabled.

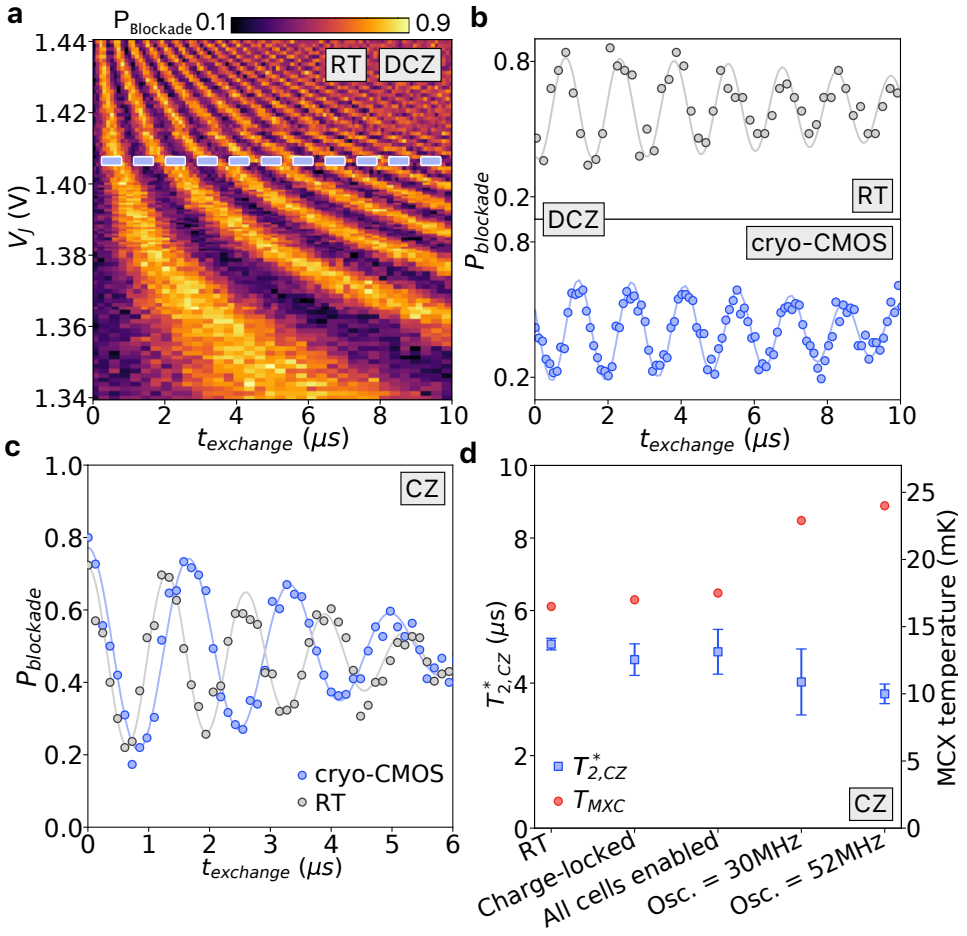

Figure 5.4: **Two-qubit operations using cryo-CMOS. a**, Decoupled controlled phase (DCZ) oscillations as a function of exchange time $t_{exchange}$ and V_J, performed using RT control. **b**, RT and Cryo-CMOS-enabled DCZ oscillations at a set V_J, indicated in a. Set level is determined by V_{HOLD}, which can be tuned for stronger qubit interaction.* **c**, Comparison of visibility between RT and cryo-CMOS control using identical pulsing methods on all gates. Increased state preparation and measurement error is present due to two-level-only approach to pulsing J. **d**, CZ coherence times of our two-qubit control conditions under various cryo-CMOS parameters. J pulses are generated by cryo-CMOS unless otherwise indicated.

5.4 Discussion

Our cryo-CMOS control chip comprises complex mixed-signal circuits realized using more than 100-thousand transistors. The vast majority of these are used in the digital sub-systems and related circuit blocks, accounting for a fixed overhead power of 10s of microWatts. On top of this constant offset power from the digital blocks, the CLFG analog cells each contribute $\sim$ 20 nW/MHz when generating 100 mV amplitude pulses, enabling many thousands of cells (and thus gate electrodes) to fit within the cooling budget of a commercial dilution refrigerator ($\sim$ 1 mW at 100 mK) [1]. Aside from the cooling limits of the refrigerator however, a challenge arises in the thermal management of hot control systems to ensure the routing of heat bypasses proximal, cold quantum devices. Here, we have made little attempt to mitigate this parasitic heating, simply wire-bonding the chips together in a standard package. This arrangement can lead to elevated electron temperatures in the quantum device (see Extended Data Fig. 5.7) even when the refrigerator remains cold and is the likely explanation for the small impact we observe in qubit fidelity when the largest CMOS circuits are powered up at the highest clock rates. As such, we emphasize that there is significant opportunity to suppress parasitic heating by employing separate parallel cooling pathways for the CMOS chip and quantum plane. The use of heterogeneous, rather than monolithic integration opens new thermal configuration options in this regard.

Beyond direct heating, the close presence of 100-thousand transistors, with volt-scale biasing and sub-nanosecond rise and fall times, can create an exceedingly noisy environment in which to operate electrically sensitive qubits. It is perhaps surprising then that we observe the CMOS chip to have only a small impact on qubit performance. Even further, the small degradation in fidelity is likely explained entirely from parasitic heating, rather than from electrical noise.* Certainly, our use of CMOS design-rules that minimize external crosstalk are important, however beyond these, we suggest three additional aspects that likely reduce electrical noise. Firstly, since the physical temperature of the CMOS die is a few-hundred milli-kelvin, thermal noise contributions are significantly suppressed. Also, the chip-to-chip interconnect likely has a relatively low bandwidth, filtering noise above a few giga-Hertz. Lastly, we note that the action of the CLFG circuits effectively decouple the CMOS from the quantum device when in charge-lock mode, except for a very small coupling capacitor. Taken collectively these aspects further underscore the utility of heterogeneous over monolithic integration for mitigating crosstalk and heating. In addition to addressing the challenges posed by scaling-up qubits, cryo-CMOS using a chiplet architecture may also prove useful in generating ultra-fast, low thermal noise control pulses that probe fundamental physics in

*An electrical noise contribution is likely still present, however it is indistinguishable from parasitic heating and possibly below the noise floor of the experiment.

mesoscale quantum devices [259].

In conclusion, the results presented here demonstrate the viability of heterogeneous, milli-kelvin CMOS for scalable control of spin qubits. Beyond addressing the interconnect bottleneck posed by cryogenic qubit platforms, these results show that degradation in qubit performance from milli-kelvin CMOS is very limited. Although our focus here has been controlling spin qubits based on single electrons, we draw attention to the inherent compatibility of our control architecture with other flavours of spin qubits, for instance, exchange only qubits that leverage square voltage pulses exclusively [36]. More generally, this architecture is likely to find utility in scaling-up other kinds of semiconductor qubits that operate using biases applied to gate electrodes [260].

5.5 Methods

5.5.1 Measurement Setup

Measurements are performed in a Bluefors LD400 dilution refrigerator with a base temperature of 7 mK. The qubit chip and cryo-CMOS chip are packaged on the same FR4 printed circuit board (PCB) [261], separated by 3 mm and wirebonded together. The daughterboard PCB is placed on a custom motherboard and electrically connected via an interposer. The motherboard manages signals from room temperature and the ESR line connects directly to the daughterboard via a mini-iSMP. The PCB setup is mounted in a magnetic field, on a cold finger. The external magnetic field is supplied by an Oxford MercuryiPS-M magnet power supply. DC voltages are generated by an in-house custom digitial to analog converter (DAC). A Quantum Machines OPX+ generates RT dynamic pulses, the 400 MHz signal for RF-readout, I/Q and pulse modulation for the MW source as well as trigger lines to the cryo-CMOS chip and MW source. Dynamic and dc voltage sources are combined at room temperature using custom voltage combiners. The OPX has a sampling rate of 1 GS/s and a clock rate of 250 MHz. The MW tone is generated by a Keysight PSG E8267D Vector Signal Generator with a signal spanning 250 kHz to 31.8 GHz. We use an RF-SET and RF reflectometry readout, comprising a Low Noise Factory LNF-LNC0.3-14A amplifier at the 4 K stage of the refrigerator and a Minicircuits ZX60-P103LN+ at RT for signal amplification. The directional coupler in Fig. 5.1 (a) is a Minicircuits ZEDC-10-182-S+ 10-1800 MHz.

5.5.2 Cryo-CMOS Programming

Our cryo-CMOS receives programming instructions, power, dc bias, and dynamic voltage levels from an in-house RT DAC [262] and is configured to receive an external trigger from the OPX+,

as well as RT dynamic pulses for passthrough RT control. Some of the programming instructions as well as the external trigger are received by the same input line. Appropriate input is handled by a Minicircuits RC-4SPDT-A18 DC-18 GHz RF switch, which takes inputs from both the DAC and OPX+. The RF switch is programmed to work in unison with charge-locking commands sent to the cryo-CMOS, switching inputs from the DAC to the OPX+ once programming is complete.

Due to the low leakage rate of our cryo-CMOS transistors, there are no charge-lock refresh cycles of our charge-locked gate when performing experiments. Maximum experiment times are approximately one hour, usually single-qubit RBM or PSD measurements.

5.6 Extended Data

The following figures present data crucial to further understanding this work. Figs. 5.5 - 5.7 detail hardware setup and specifications, as well as operation methods. In addition, Fig. 5.7 presents more temperature dependency data using both cryo-CMOS and MXC chamber heating. Figs. 5.8 and 5.9, on the other hand, present more single- and two-qubit data as a function of various cryo-CMOS parameters. Exploration of coherence times as a function of divided frequency and oscillator frequency is explored in more detail.

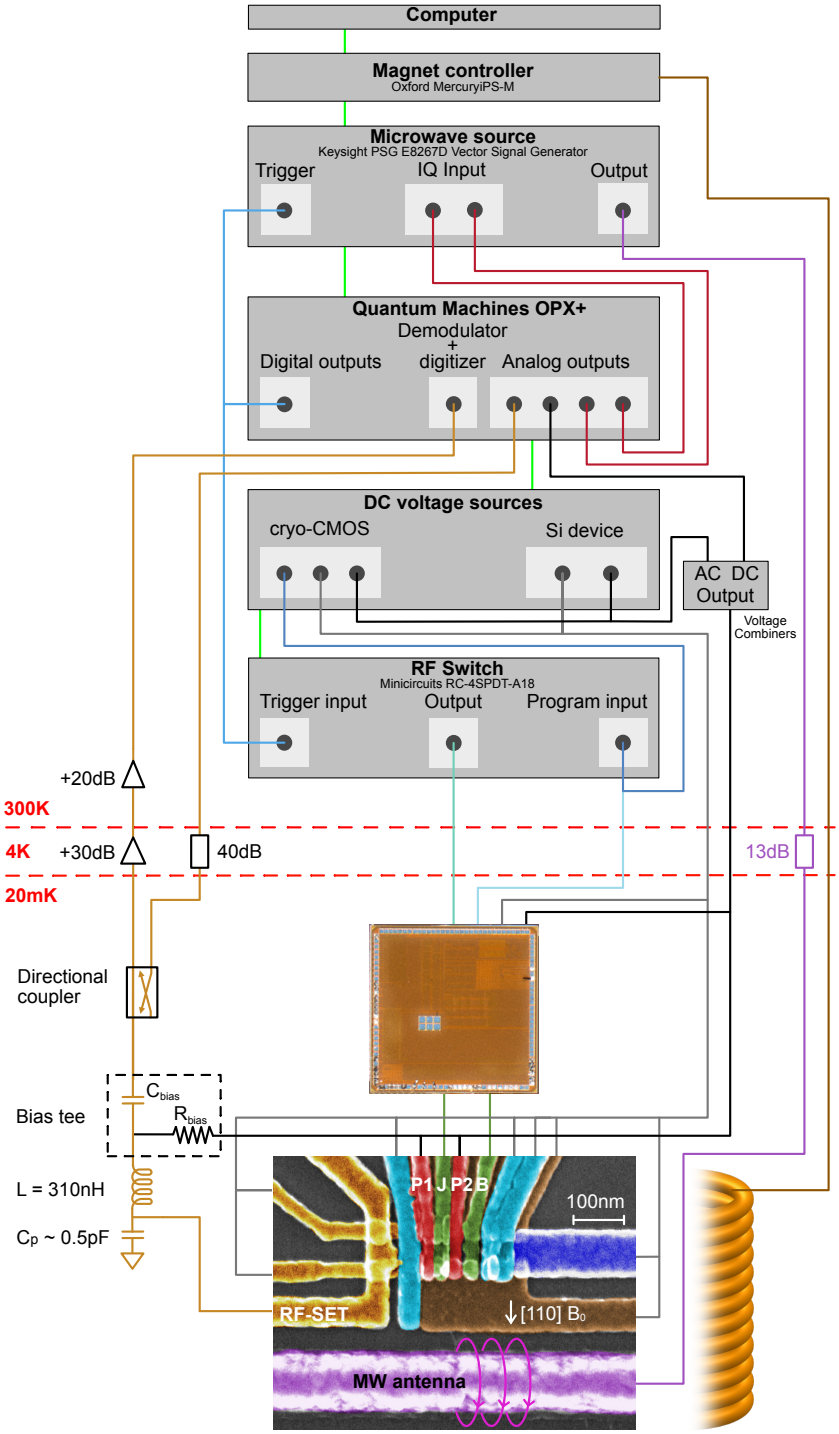

Figure 5.5: **Full experimental setup.**

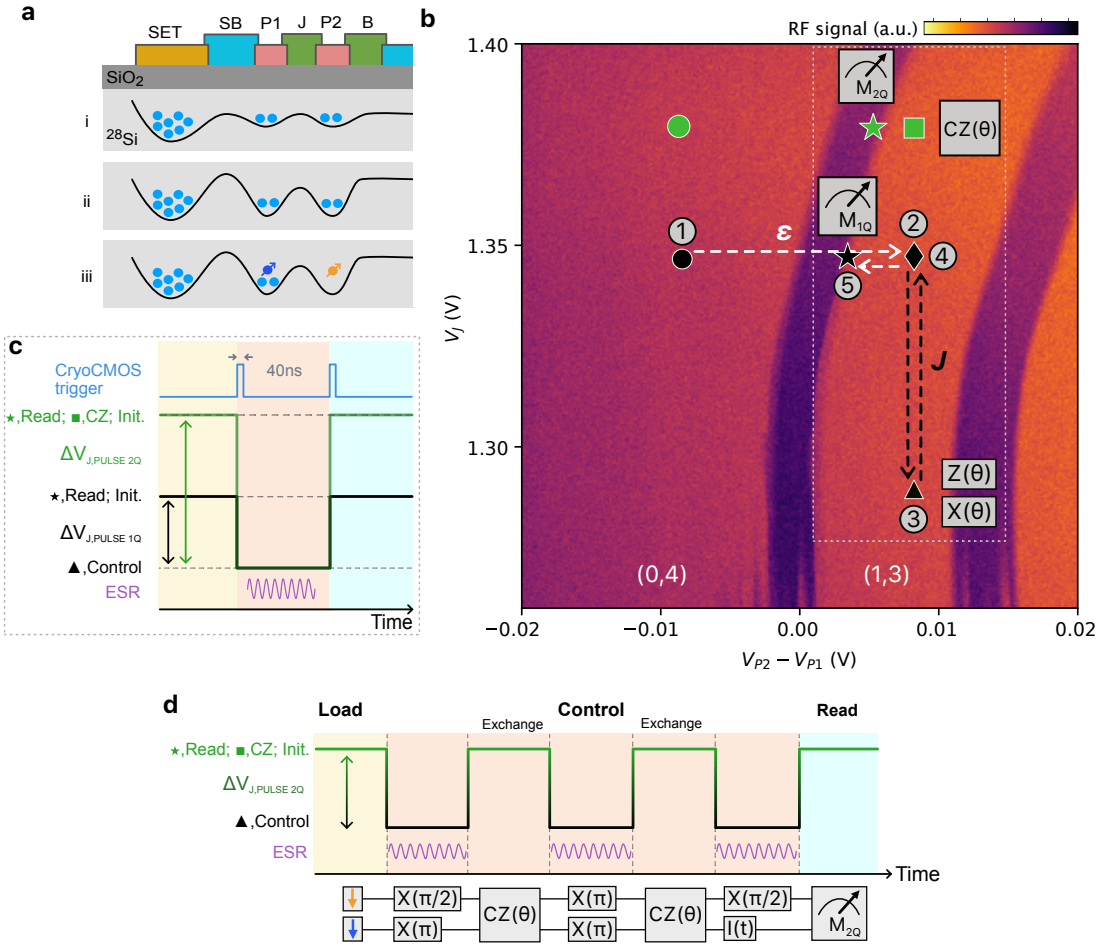

Figure 5.6: **Loading and pulsing scheme.** **a**, the barrier to the SET reservoir is lowered for a set number of electrons to occupy the dots (i). This barrier is raised to isolate the dots (ii), and the electron states are initialized via tuning of the plunger gates P1 and P2 (iii). **b**, Single-qubit pulsing scheme for ESR measurements. A diabatic detuning ramp $(1 \rightarrow 2)$ from the (0,4) to (1,3) state initialises the double quantum dot into a singlet state. The qubit is then pulsed using the J-gate to the control point $(2 \rightarrow 3)$ at which point a MW pulse is applied that rotates the target qubit in resonance with the MW frequency. The qubit is pulsed back to ♦ $(3 \rightarrow 4)$, then pulsed into the Pauli Spin Blockade regime $(4 \rightarrow 5)$ for readout. Detuning ϵ pulses use gates $P1$ and $P2$ and are always RT-operated. J-gate pulses are generated either at RT or by cryo-CMOS. The approximate operation points of single qubit (X, Z), two qubit (CZ), and readout points (M_{1Q}, M_{2Q}) are indicated by a triangle (▲), square (■), star (⋆) and diamond (♦) respectively. **c** (inset of b), basic J-gate pulsing scheme for ESR measurements when using cryo-CMOS. Here, the gate J is in a "charge-locked" state held at V_{HOLD}. An external trigger is used to pulse between the two J-gate levels, whose separation is determined by $\Delta V_{J,PULSE}$. **d**, DCZ sequence focussing on J-gate pulses. The qubits are initialised into a T_- state, before X and $X/2$ gates are performed on the control and target qubits respectively. A spin-echo sequence is inserted between the exchange gates, which precedes the final projection for measurement of the two-qubit spin state.

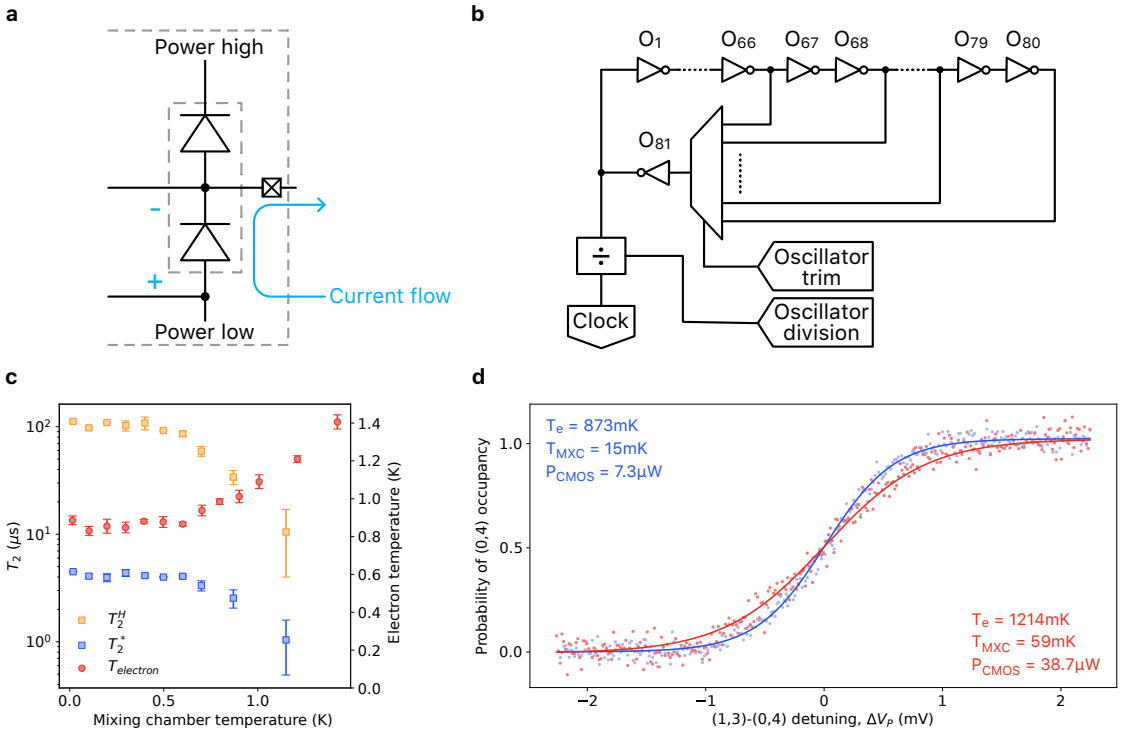

Figure 5.7: **Temperature dependence using artificial cryo-CMOS and mixing chamber heating. a**, By forward biasing an ESD protection diode on-chip, the power draw can be programmed to mimic that of any oscillator trim or division value upon oscillator activation. Artificial power draw also allows for higher resolution investigation versus other parameters, as well as extrapolation beyond what the maximal cryo-CMOS power draw possible with it's feature set. **b**, Schematic of the cryo-CMOS ring oscillator. 81 in-series inverters are connected to a three-bit multiplexer, controlling the tap-off point. The frequency is tunable by programmable inputs into the oscillator trim. This frequency is further divided by the oscillator divider, which is eight-bit tunable. The ultimate output frequency is then passed on to the FSM. **c**, Hahn echo coherence time and Ramsey coherence time of Q1, and measured electron temperature as a function of mixing chamber temperature. Base effective electron temperature is approximately 850 mK, which only starts to increase once the mixing chamber exceeds 700 mK. Electron temperature and mixing chamber temperature equalize at 1 K **d**, (1-3)-(0,4) charge occupation probability. Solid lines are Fermi distribution fits, allowing for extraction of effective electron temperature. Fitting to distributions with high mixing chamber temperature (at which point becoming equal to that of the sample) allows for determination of the lever arm.

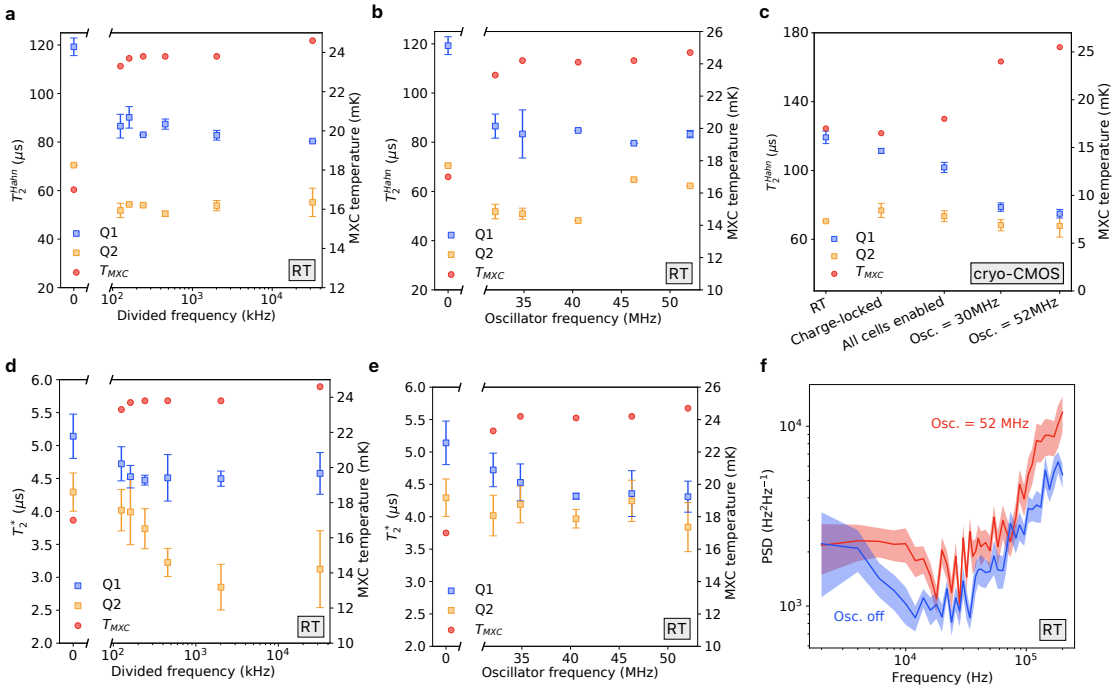

Figure 5.8: **Extended single qubit performance. a**, T_2^{Hahn} coherence of both qubits as a function of divided frequency from the cryo-CMOS oscillator. The output clock frequency (here set to 30 MHz) passed to the fast state machine is divided by an integer between 1 and 255, see Extended Data Fig. 5.6 for schematic details. The inset indicates whether RT or cryo-CMOS control is used; all RT pulsing schemes are replicable by cryo-CMOS. Activating the oscillator immediately causes a drop in coherence due to the extra thermal dissipation, and lowering the divider value increases this dissipation slightly. **b**, Qubit coherence while directly changing oscillator frequency. The divider is set to a constant value of 255, and increasing oscillator frequency leads to an increase in power draw of the cryo-CMOS chip, reflected in the mixing chamber temperature. **c**, Similar to Fig. 5.2 (c), T_2^{Hahn} coherence is also explored as a function of various parameters under cryo-CMOS control conditions. **d, e**, T_2^* of both qubits while changing the divided and oscillator frequencies, similar to a and b. **f**, The noise power spectral density (PSD) is explored as a function of oscillator frequency. Noise spectroscopy, based on the Carr-Purcell-Meiboom-Gill (CPMG) protocol [263–265], uses a single qubit as a noise probe. A rise in the overall white noise level over the detectable frequency range when the oscillator is at its maximum frequency is observed. At higher frequencies, we observe an increase in PSD, likely due to high-power driving or miscalibration of microwave pulses [250, 266, 267].

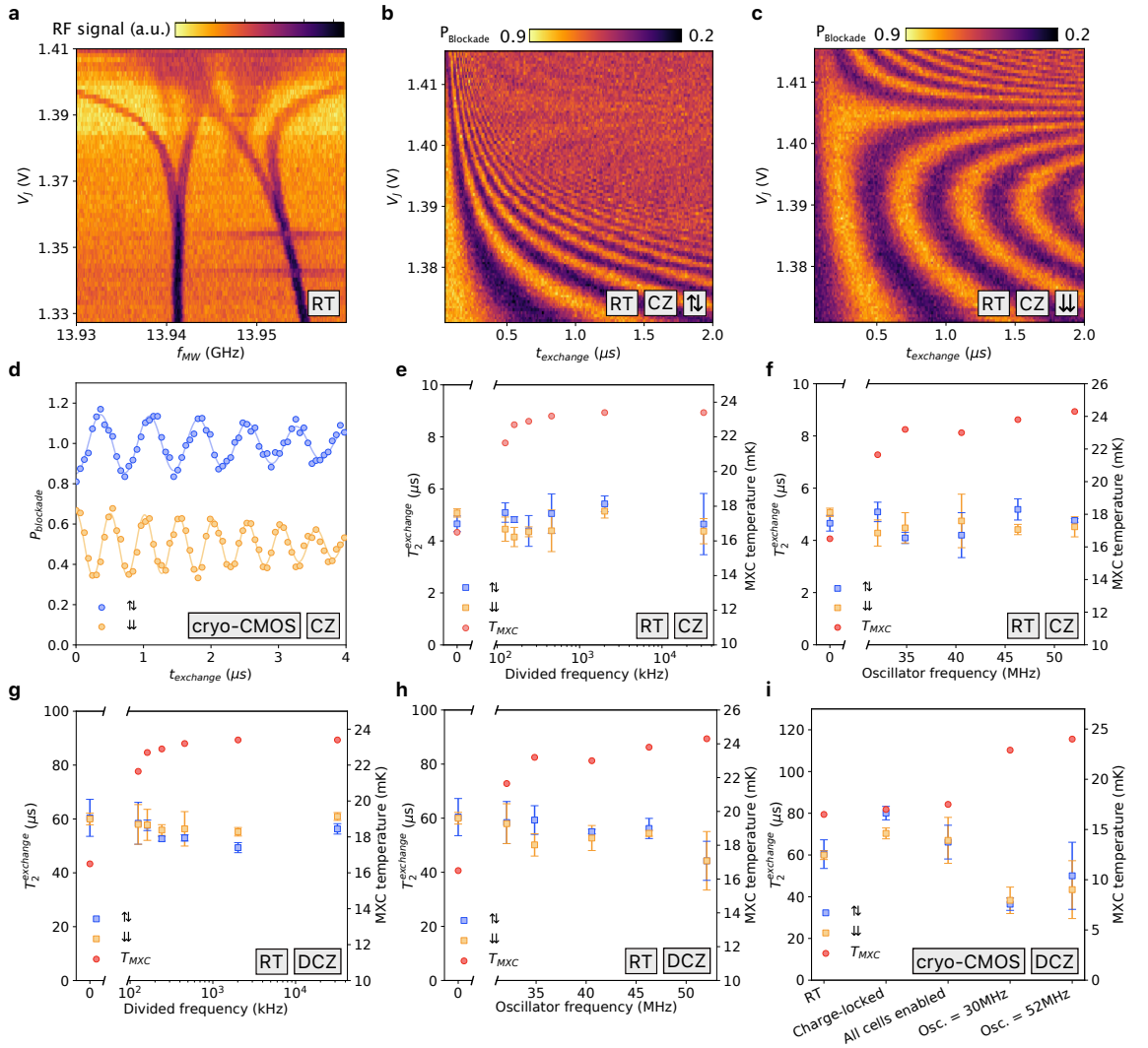

Figure 5.9: **Extended two-qubit performance and dependence on cryo-CMOS parameters.** **a**, ESR spectrum as a function of V_J. Exchange starts to open at around V_J = 1.37 V. Measurements are done with room temperature J pulses; RT or cryo-CMOS control is indicated in the lower right hand side of each figure. **b, c**, CZ oscillations as a function of exchange time $t_{exchange}$ and V_J. Multiple J levels, not replicable by cryo-CMOS control are used here for optimal performance. The initial state of the target control qubits is indicated in the bottom right hand corner. **d**, CZ oscillations using cryo-CMOS control, showing the difference in visibility compared to **b-c**. Traces are offset for clarity. For all further figures, pulses are two level and if generated at RT, are replicable by cryo-CMOS. **e**, similar to Extended Data Fig. 5.8 (a), the two qubit CZ coherence time $T_2^{exchange}$ is explored as a function of divided frequency. The oscillator is set to 30 MHz for all divisions, and pulses are generated from room temperature. **f** CZ coherence time $T_2^{exchange}$ is now explored as a function of oscillator frequency. The divider is set to 255 for all measurements. **g, h**, Measurements in **e, f** are replicated here, however now using a DCZ pulsing protocol, allowing for longer coherence times. **i**, DCZ coherence is explored using cryo-CMOS control under various parameters, similar to Fig. 5.4 (d).

5.7 Acknowledgements

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6

Conclusion

The last decade has seen significant investment in and demand for quantum computing systems. The advent of single- and two-qubit gates in multiple architectures surpassing the error-correction threshold [189, 268–271] has prompted researchers and organizations to pursue the immediate scale-up of these systems. At the time of writing, ~ 1000 qubit systems have been built using brute force approaches, without implementation of efficient control and readout mechanisms. Such an approach for millions of qubits is incompatible with cryogenic systems, and will require the use of next-generation control and readout technologies.

This thesis explores scalable readout and control technology compatible with condensed-matter-based approaches to quantum computation, with experimental findings detailed in Chapters 4 and 5. In Chapter 4, the focus lies on the presentation of dispersively sensed Aharonov-Bohm phase data, which tackles both qubit architecture and readout efficiency. The primary objective of this experiment is to demonstrate the compatibility of this readout technique with topological-based systems, a notion further substantiated by recent research on dispersively sensing fermion parity [272]. Dispersive readout techniques on their own have been implemented in many separate architectures [88, 91, 273], offering the promise of reducing the total footprint of the quantum systems by removing the need for discrete charge sensors. Chapter 5, on the other hand, showcases the coherent control of spin qubits through a co-located scalable CMOS architecture. This proof-of-concept paves the way for controlling millions of qubits locally, thereby significantly reducing the number of I/O channels between milli-kelvin and room temperature systems.

6.1 Topological Architectures

The prospect of encoding quantum information onto topological properties holds the promise of significantly mitigating qubit noise, as quantum information becomes shielded from local environmental perturbations. Unlike spin-based approaches, which are susceptible to the influence of a noisy environment, topological systems remain largely unaffected, potentially resulting in physical qubits with markedly higher fidelities. Consequently, the journey towards realizing logical qubits becomes considerably shorter, as fewer physical qubits are required to encode a single logical qubit. This topological approach, compelling for some research organisations [274–276], comes at the cost of increased device complexity. The physics underlying the topological protection of quantum states also renders the control and readout of these states particularly challenging. Presently, only two platforms are known to host non-abelian anyons: fractional quantum Hall states [277] and Majorana fermions. Realising an anyon-based qubit is a formidable engineering challenge, requiring fabrication techniques learned from other architectures and employment of a measurement-only approach (dispersive sensing) to bypass some of these obstacles. Still, this increased complexity means that at the time of writing, however, no qubit statistics have been reported.

6.2 Scalable Readout Techniques

Readout will soon prove to be a limiting factor in the scale-up of quantum systems. A single lumped-element circuit is thousands of times larger than quantum-dot-based qubits, and the footprint as well as power consumption of millions of readout lines is not possible to accommodate with current cryogenic systems. Dispersive readout, coupled with with other novel readout technologies will alleviate this issue. The crux lies in increasing the number of charge sensors per readout channel. Techniques such as frequency multiplexing [9], time division multiplexing [10], orthogonal frequency division multiplexing, and other CMOS-based readout methods [11] offer avenues for reducing the sensor-to-readout-chain ratio.

The fusion of frequency and time-division multiplexing alone may open up the possibility of using a single readout line for tens of thousands of charge sensors. Fig. 6.1 illustrates the hardware required for both techniques. In currently unpublished work, I explored time division multiplexing in GaAs systems that share the same lumped element circuit, readout channel, and source ohmic to sense their local environment sequentially using fast on-chip switches. Each of the eight QPCs in Fig. 6.1 (c) connect to a single source ohmic, via eight output paths. Six addressing gates

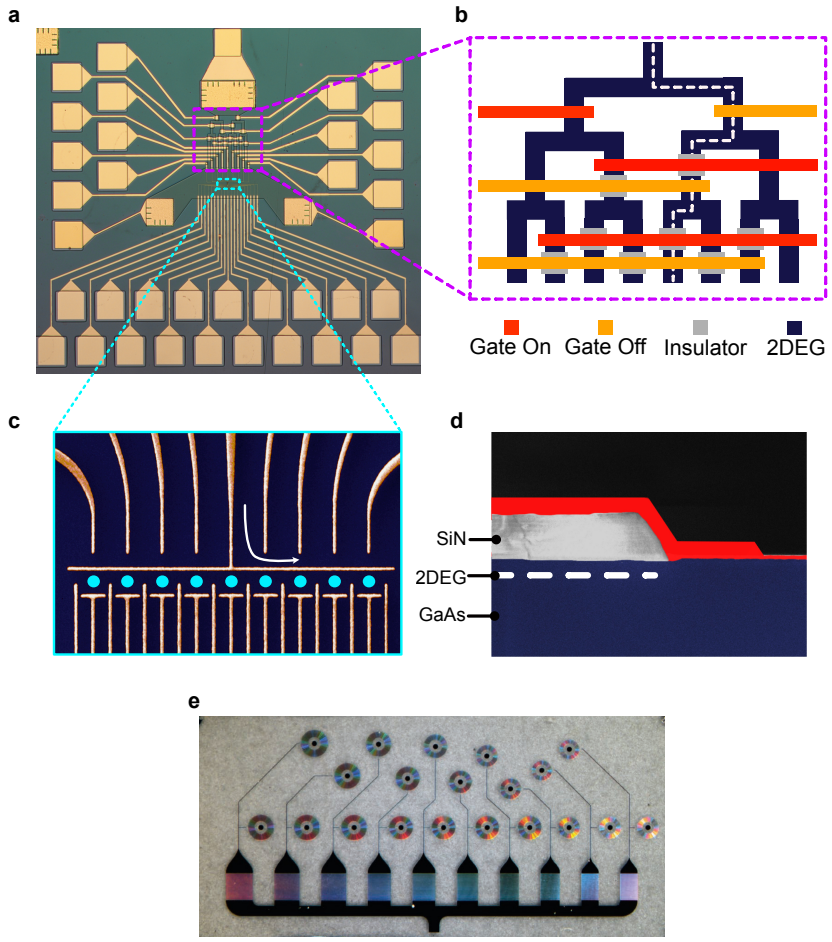

Figure 6.1: **Frequency and time-division multiplexing. a**, A nine quantum dot device featuring eight quantum point contacts that share a single source ohmic. **b**, Each quantum point contact is connected to the source ohmic read out sequentially by activation of channel barrier gates. This particular design allows for efficient scale-up between the ratio of channel number to barrier gates. **c**, False color micrograph of the nine-quantum dot device. The activated quantum point contact (arrow indicating current flow) corresponds to the connected channel in (b) **d**, Side profile of a barrier gate deposited on top of an SiN layer. The 2DEG is insulated from the electric field of the gate, allowing free flowing electrons to exist in the 2DEG at highly negative gate voltages. Where the gate meets the surface of the GaAs/AlGaAs substrate, electrons are driven out. **e**, A frequency multiplexing resonator featuring multiple inductors of different values to target unique frequencies. Image reproduced from [9].

(Fig. 6.1 (b)) dictate which path is open, thereby determining the connected QPC. Turning on and off various addressing gates changes the open path by forming a barrier at the spots where the gate directly meets the GaAs substrate. Combinations of these addressing gates allow for connection to each of the QPCs [278]. This dynamic switching mechanism, with nanosecond switching times

[11], circumvents power dissipation and parasitic capacitance issues associated with CMOS switch matrices. Furthermore, fast readout (greater than 1 μs) relative to long T_1 times in silicon (approximately 500 ms) extends the utility of a single readout chain to thousands of sensors before signal degradation occurs.

Leveraging frequency multiplexing techniques further enhances readout scalability through simultaneous readout of up to 100 qubits at separate frequencies. Bonding charge sensors to separate impedance matching networks with different inductance values leads to a set of unique resonant frequencies corresponding to each sensor. Frequency spacing limits the total frequency count given by the $\sim$ 10 MHz frequency bandwidth of each readout signal compared to the maximum readout frequency of $\approx$ 1 GHz.[1] Employing orthogonal frequency division multiplexing will increase this number as carrier frequencies can be spaced closer.

6.3 Local Control of Qubits

Chapter 5 presents work demonstrating coherent control of qubits at milli-kelvin temperatures using a proximal CMOS chip for the first time. Local, milli-kelvin control has been proposed using various methodologies [1, 5, 11, 279, 280], however, to-date how it affects qubit fidelity has remained an open question. While cryo-CMOS control does not change the number of control lines per qubit (arguably it increases slightly), it addresses the fundamental room-temperature-to-milli-kelvin bottleneck caused by the cooling power and footprint of a cryogenic fridge. Cryo-CMOS acts as the baseband pulsing source through the use efficient analogue circuits (Fig. 5.1), necessitating only power, digital I/O and some DC lines to occupy fridge space.[2] This is a considerable gain, eliminating all the high frequency gate pulsing lines that for thousands of qubits cumulatively dissipate potentially watts of power. To drive ever shorter sub-nanosecond pulse lengths over two meters of coaxial cable comes at the cost of increased power dissipation and noise temperature due to in-line losses, costs which are virtually eliminated when using proximal analogue switches. The adoption of CMOS manufacturing methods for compatible silicon processors in particular will produce consistently high-quality quantum devices as well as novel lithographically-defined interconnects between classical and quantum systems [12, 13, 281]. The ability of the SiMOS architecture to achieve high fidelities at elevated temperatures [248–250] reduces practical scalability concerns in commercially available dilution refrigerators. Further, this addresses the long concerns of scale-up, eliminating the immediate need for enormous dilution units [282] and expensive cryogens.

[1] At higher frequencies (shortened wavelength) the circuit can no longer be treated as lumped element.

[2] Depending on architecture, certain MW lines may also be necessary.

Future iterations of this experiment should incorporate several improvements based on observations made during this study. These enhancements can be categorized into four main areas: fridge setup, cryo-CMOS ASIC design, device architecture, and thermal considerations.

One of the first changes to dramatically reduce total circuit time is to DC-couple all lines. The settling time, even when compensating pulses are employed, constitutes the majority of shot times in all cases. The elimination of settling time would not only make it possible to execute longer circuits but may also result in slight visibility improvements due to the reduced ratio of shot time to T_1. In addition, implementing a better-matched readout amplifier and a more sophisticated readout chain (such as the inclusion of a parametric amplifier on-chip [32] or similar, and a cryo-ADC [33]) can enhance readout signal-to-noise ratio (SNR) or conversely further reduce readout time. Finally, there are multiple techniques to reduce noise within the system, such as replacing the superconducting solenoid with a permanent magnet, and custom SMA lines for reduced triboelectric noise.

Advancements in cryo-CMOS ASIC design are expected to progress rapidly, possibly surpassing the immediate needs of qubits. Of the host of possible improvements, I believe there are several easy pickings that will substantially aid in future experimental work. Having only two voltage levels when under cryo-CMOS control severely limits the ability to optimise or even execute certain quantum circuits. Introducing at least four voltage levels for any particular gate should alleviate this constraint.[1] Better communication via the serial peripheral interface and a more versatile register and oscillator are necessary, allowing gates to be controlled using internal triggering protocols, and enabling on-demand reconfiguration of the cryo-CMOS. A lower power density, and possibly multiple chips for distributed computation at different cooling power stages will help combat the thermal issues experienced. An on-chip temperature probe, and multiple distributed temperature probes [283] are also needed to understand the thermal gradients present under operation.

One of the major concerns arising from this experiment is thermal output and mitigation. In Chapter 5, the cryo-CMOS and Si chips are mounted on the same PCB with no specialised thermal mitigation present. This represents a 'worst case' scenario in the short term, as such mitigation techniques are easy to implement. Better thermal anchoring to the mixing chamber is required, as a relatively small change in mixing chamber temperature lead to outsized impact on the electron temperature (Fig. B.12), indicative of poor thermal connectivity between the two regions. Thermal isolation between the cryo-CMOS and qubits is essential to further reduce the electron temperature. With these measures in place, I'm confident that electron temperatures can be brought down to approximately 200 mK, limited by other factors such as quantum dot size and microwave heat-

[1] Gates will eventually need to share levels, otherwise we run into the same scalability concern that necessitates the use of cryo-CMOS.

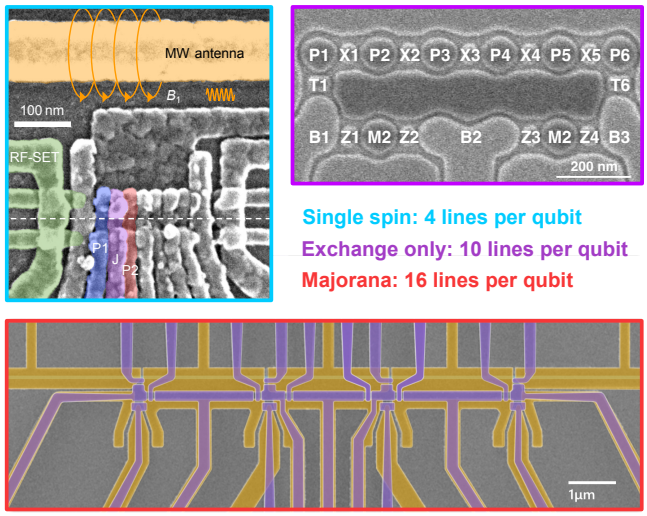

Figure 6.2: **Control lines per qubit.** Each architecture makes tradeoffs in the number of control lines per qubit for separate scalability benefits. Single-spin qubits require fewer lines, but need a high frequency microwave line to rotate spins. Exchange-only systems need three quantum dots to create a single qubit, using the exchange interaction only (baseband pulses) for qubit control. Majorana-based approaches require significantly more control lines for potentially much higher fidelity rates. Figures reproduced from [36, 250, 272] respectively.

ing rather than cryo-CMOS presence.

Despite the numerous necessary improvements, the capability of the cryo-CMOS used in this work suggests that there is immediate room for scaling without any changes. Controlling the majority of gates cryogenically is an obvious goal for future experiments, as well as controlling other qubit systems. Architectures using voltage-based approaches are compatible with this technology, including but not limited to atom-phosphorus, carbon nanotube, Si/SiGe, nuclear spin, and many other quantum-dot-based systems. I think we will see significantly more demonstrations with these in the years to come.

There is a sweet spot in the fidelity-temperature scale, at which all qubit architectures can operate most efficiently cost-wise. For Si spin qubits, that point is likely around 1.1 K, which means with the improvements I've detailed in place, there is opportunity for control of thousands of qubits before commercial fridge cooling power becomes a concern. This experiment, I believe, also puts to rest the ongoing debate of whether monolithic [13] or chiplet-style [12] integration is better. Even with a cryo-CMOS chip a few mm away, the electron temperatures still soared. Barring revolutionary ASIC advancement, placement of hot electronics microns from the quantum dots will likely prove fatal to their fidelities.

6.4 The Tyranny of the Final Product

The title of this final Section draws inspiration from William Zinsser's *On Writing Well* [284], where he explores the dichotomy between quest and intention in the writing process. Similarly, my doctoral journey can be dissected into these two fundamental concepts. Experiments, like writing, rarely follow a linear path, often finding intention and quest in conflict. Intentions, encapsulating the initial ideas and the dissemination of results, guide the overarching goals of my work. Chapters 4 and 5, for instance, are driven by the intention to demonstrate more efficient utilization of qubits. Distilling a coherent narrative from the vast and tangled mess of individual measurements, however, is challenging. Complicating matters is the relentless pursuit of just *one more thing* — the quest inherent in experimentation. This pursuit for additional data leads to unexpected insights, radical new ideas and sometimes outright failure.[1] Appendices A through F serve as chronicles of these quests, showcasing results and methodologies vital to the realization of the final narrative but not necessarily part of it.

Beyond my individual journey, the broader quantum computing community follows a similar trajectory. The intention has always been to construct a fault-tolerant, general-purpose quantum computer. The quest has spawned dozens of unique architectures, deepened our understanding of fundamental physics, catalyzed advancements in diverse scientific domains, and sparked countless secondary societal impacts. Just like with classical computing systems, the quest will never be over in our grand intention to answer ever more questions.

[1] Time division multiplexing mentioned earlier is an example of one of these failures. I was never able to fabricate and measure a fully functioning device, and ultimately made the decision to move on. See appendix C.

Appendices

A

Additional Material for Fast Detection of the Aharonov-Bohm Phase with Gate Reflectometry

Extra details of device design, and results not included in the body chapter are detailed here, aiding in analysis of device behavior. These include extraction of critical 2DEG statistical behavior via a Hall bar, tuning characteristics of both devices and analysis of universal conductance fluctuations. Finally, future experiments are proposed to help realize a MZM-based architecture.

A.1 Hybrid Design Approach

AB rings typically use a single confinement method for definition and control. In this experiment, two confinement methods are used: electrostatic confinement defines the outside of the ring, and etched confinement the inner portion. An electrostatic-only approach is ideal; however, we believed that the large metallic island defining the inner ring may act as a capacitive shunt to ground, leading to no useful dispersive data. A semi-hybrid approach was also considered, where small portions of the inner ring were electrostatically controlled for better dot definition. Cleanroom expertise and capability of sub-micron air-bridge fabrication ultimately prevented this approach.

Multiple fabrication and measurement tests revealed that the defined inner etch ring size and the actual measured radius (via AB effect) can vary up to 30%. This restricted the range of possible designed ring sizes, as straying close to the Fermi wavelength could result in extra interference

Density	$1.35\ m^{-2}$
Mobility	$12.45\ m^2V^{-1}s^{-1}$
Mean free path	$755\ nm$
Fermi wavelength	$68.3\ nm$
Fermi wave vector	$9.19 \times 10^7\ m^{-1}$
Fermi velocity	$1.59 \times 10^5\ ms^{-1}$
Fermi energy	$0.0123\ eV$

Table A.1: Important 2DEG values for analysis the Aharonov-Bohm effect and ring design.

effects, and approaching the phase-coherence length may inadvertently destroy the phase information. Each measured device is designed to contain multiple conduction channels (up to 10) to accommodate for the error in fabrication.

A.2 Hall Bar Analysis

Hall bars are included on all GaAs devices to understand the characteristics of the 2DEG. A more detailed overview of Hall bar analysis is in Section 2.2, here I detail results solely from this experiment. On both devices a number of Hall bars are included as 2DEG characteristics varied across the two inch wafer. Over the 4x4 mm chip size, except near one edge where the 2DEG ceases to exist (located at the edge of the wafer), no significant deviation in values were observed. Fig A.1 shows an image of a Hall bar on chip, as well as Schubnikov-de Haas oscillations observed at higher field values.

A.3 Device Tuning

The second device presented in the main work was originally meant to form a dot within the AB channel. Due to a combination of initial design and fabrication outcomes, forming dots proved near impossible. Instead, a QPC-sensing method is used. The wall gates intended to define the quantum dot electrostatic barriers help tune the QPC for maximum sensitivity. QPCs typically use two opposing gates to form the 1D channel, however here one gate defines a channel against a rough edge wall of the inner AB ring. This 1D channel therefore is more chaotic with varying channel width and formation dots at random sites. Evidence of quantization is clear with sensitivity capable of AB phase detection. The tuning for maximum sensitivity is different for RF and DC readout methods.

Similarly, unlike traditional quantum-dot devices, forming a dot against the rough edge wall is

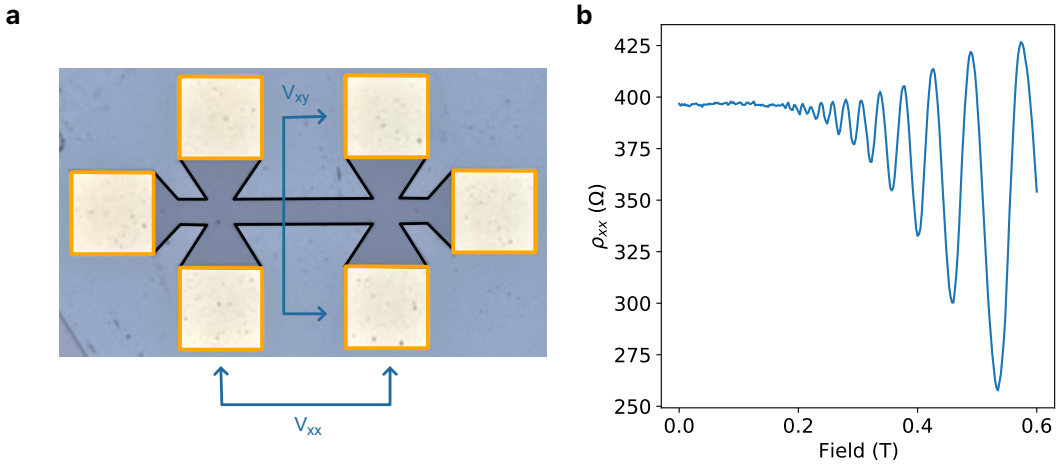

Figure A.1: **Hall bar and Schubnikov-de Haas oscillations. a,** Microscope image of a Hall bar on-device, with the measurements V_{xx} and V_{xy} indicated on the corresponding ohmics **b,** Schubnikov-de Haas oscillations are observed at higher perpendicular magnetic field values, and have a period proportional to 1/T.

difficult. There are fewer ways to manipulate the shape and size of the dot, possibly reducing the maximum possible sensitivity of the sensor. Dot formation in the first device presented is acceptable, but presents some abnormal behaviors. Asymmetry in both devices is present due to deviations in the etching of the inner AB ring. Fig. A.2 shows tuning behavior of both devices, featuring dots, Coulomb blockade and pinchoff behavior. The comparison demonstrates the magnitude of which small design and fabrication changes can affect outcomes.

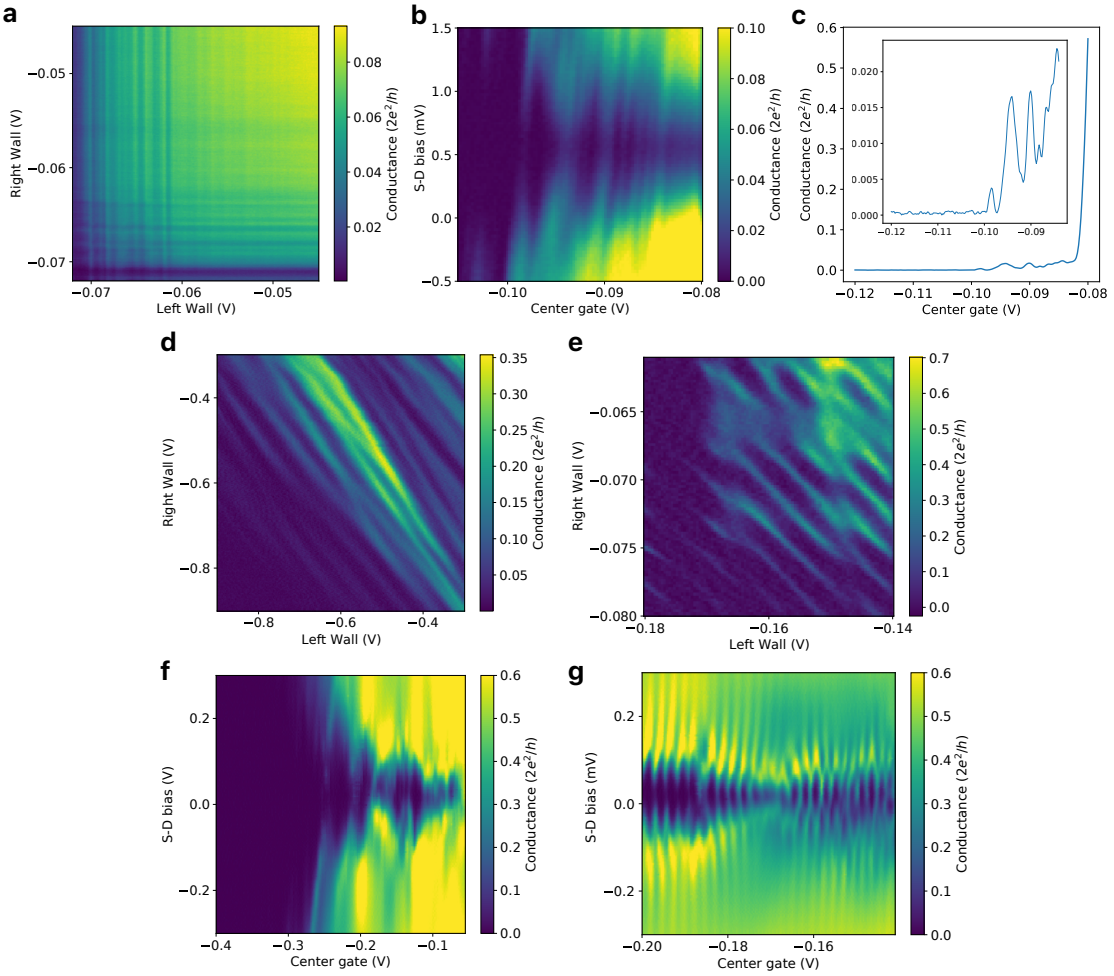

Figure A.2: **Quantum dot behavior of both tested devices. a,** Failed dot formation as a function of the two wall gates. Device two is unable to form acceptable quantum dots for charge sensing. The gates are likely too close to the etched side wall of the inner AB ring. **b,** Coulomb diamonds indicate that there is some dot formation present, however it is inadequate for the purposes of sensing the AB phase. **c,** The pinchoff profile is abrupt, meaning that the channel closes very quickly. Inset: zoom in of the QPC sensing region. The pseudo-Coulomb peak is used as a sensitive charge sensor, similar to how traditional QPCs use the rising edge of quantized conductance. **d,** Dot formation of the top dot on device one. This dot is much better compared to device two, but still shows some unusual features due to the lack of electrostatic confinement for part of the dot. **e,** Dot formation for the bottom dot of the same device. This dot was is better, and is used as the charge sensor. Despite this device visually looking symmetrical, asymmetries etch profile likely lead to the difference in dot behavior. **f,** Coulomb diamonds corresponding to the dot in d. These diamonds are better than in b, but lack the regularity expected for typical quantum dots. **g,** Coulomb diamonds corresponding to the dot in e. The dot is well defined and coulomb diamonds much more regular. There was no need for this dot to be tuned into the single electron regime, instead it was left with multiple electorns for enhanced charge sensing.

A.4 Universal Conductance Fluctuations

Beyond AB and SDH oscillations, universal conductance fluctuations (UCF) present as random fluctuations in field observed both in RF and DC. Many experiments involving mesoscopic conduction [285] have shown seemingly random yet repeatable fluctuations, that vary significantly from sample to sample and tuning to tuning. These have also been shown to increase at lower temperatures [286] and have a consistent fluctuation amplitude independent of conduction value. This is different to typical random fluctuations in conduction due to thermal noise, phonon noise, or shot noise. All these involve a temporal component, which is not the case in here as UCF is (almost) time independent.

The mechanisms that determine the presence and magnitude of UCF are the same that give rise to the quantum Hall effect, AB transport and SDH oscillations i.e. phase coherence, ballistic and diffusive transport, and mesoscopic conductance. Similar to the AB effect, for UCF to exist the phase coherence must be preserved through the length of the conduction channel of the device.[1] Unlike the AB effect, however, UCF demands a diffusive transport regime. This means that the phase coherence length L_ϕ is greater than the path length of the conductor L, and the path length is significantly larger than the mean free path l_e such that

$$l_e \ll L < L_\phi \tag{A.1}$$

In this regime elastic scattering is dominant. Inelastic scattering sites must still remain low to preserve phase information.

Path differences of conductors lead to slight changes in phase, which interfere to determine the total current. This current (and therefore conductance) is sensitive to changes along the path due to magnetic and electric fields, and changes in the locations of the scattering sites. Nominally identical samples feature variation in UCF, due to the different configuration of scattering sites through the conducting channel. Achieving near identical device performance requires significant reduction of scattering sites to enter the ballistic conduction regime.

[1] This serves as a good sanity check, if there is no AB effect and no UCF, perhaps phase isn't being conserved.

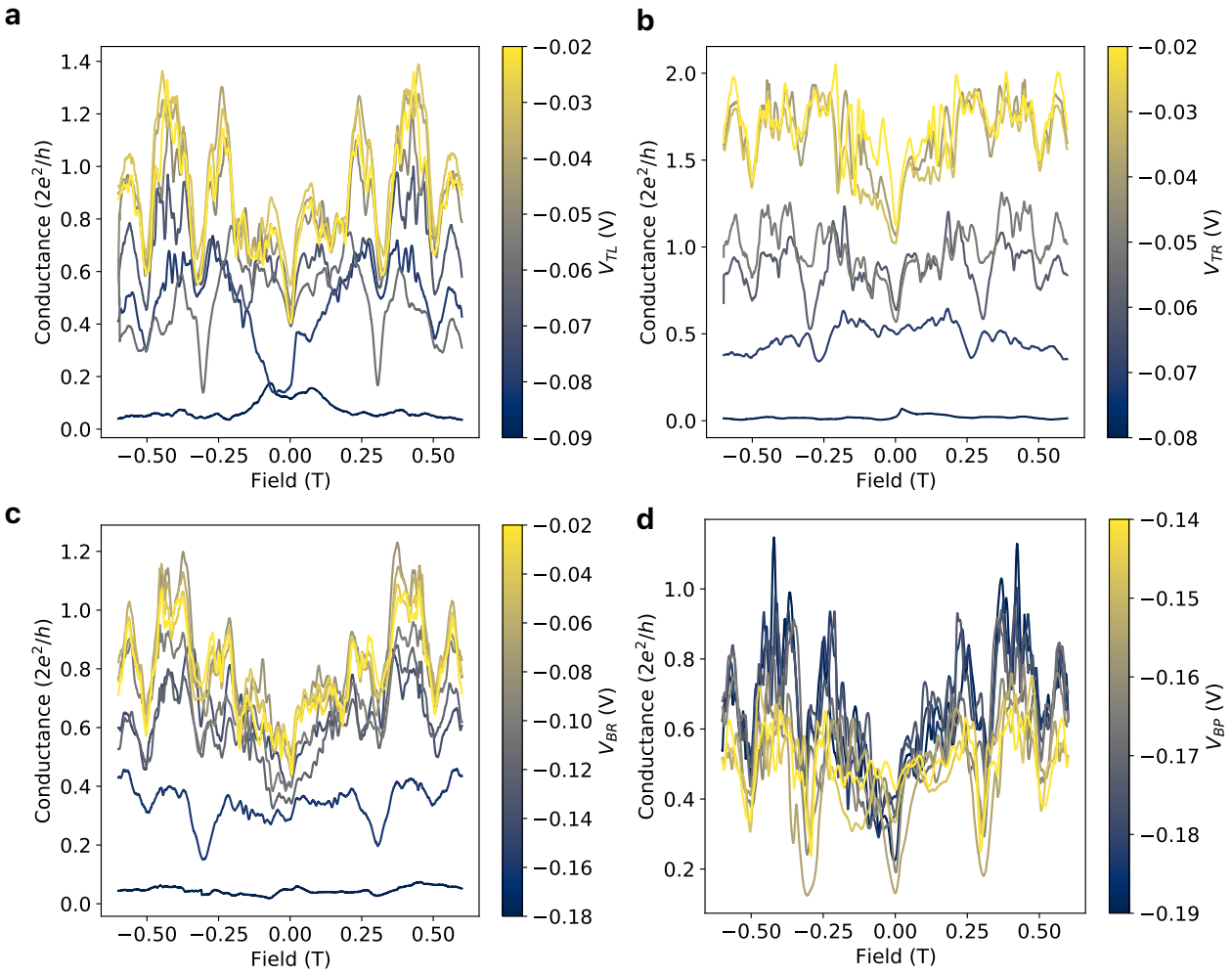

Figure A.3: **UCF as a function of field and gate voltages.** Various gates defining the top and bottom dot are swept, and the conduction through the AB ring as a function of field measured. Certain large UCF peaks are evident in all four plots, however the exact value depends on device tuning and the target gate voltage. Except for (d), all figures show a lift in conductance with a smaller gate voltage, as the channel width is increasing. Gate BP is a plunger gate with a different topology, and restricts the channel over a larger area, changing the position of eletrostatic scattering sites in a different fashion. It is not swept to its pinchoff voltage unlike the other gates featured here.

A.5 Weak Localization

Fig. 4.2 (a) presents data showing weak localization of electrons at zero magnetic field. This phenomenon is intricately linked with the Aharonov-Bohm effect, and is one of many expected to arise as a function of magnetic field, like the AB, SDH, and UCF phenomena.

An electron travelling in two dimensions within the diffusive transport window is likely to be elastically scattered a number of times by lattice imperfections and impurities contained within the conducting medium. In zero magnetic field, electrons on average are coherently backscattered such that their path start and end points are in approximately the same place. These electrons are considered weakly localized. The wavefunction of an electron with a number of possible paths arriving at a specific location is:

$$\begin{aligned} \Psi_{\text{path}} &= \sum_i \psi_i \\ &= \sum_i t_j e^{i\phi_i} \end{aligned} \tag{A.2}$$

where Ψ is the amplitude of a certain path, t is the transmission coefficient and ϕ_j, the phase evolution along the path. The probability is therefore:

$$\begin{aligned} P_{\text{path}} &= \left|\Psi_{\text{path}}\right|^2 \\ &= \sum_i t_i^2 + \sum_{i \neq j} t_i t_j \cos(\phi_i - \phi_i) \end{aligned} \tag{A.3}$$

where the first term is the probability of an electron travelling along a path j and the second is the phase interference between pairs of paths. Phase accumulation is random, leading to a cancellation of the second term.

Two symmetric electron paths can be considered time-reversed variants of one another, i.e. clockwise $(i+)$ and anti-clockwise $(i-)$ propogation around the same path. The symmetrical phase differences and corresponding amplitudes give the probability:

$$\begin{aligned} P_{\text{localized}} &= \sum_i t_{i+}^2 + \sum_i t_{i+} t_{i-} \cos(\phi_{i+} - \phi_{i-}) \\ &\quad + \sum_i t_{i-}^2 + \sum_i t_{i-} t_{i+} \cos(\phi_{i-} - \phi_{i+}) \\ &= 4 \sum_j t_j^2 \end{aligned} \tag{A.4}$$

The probability of an electron returning to its initial position is greater than any other path.

Conductance under a weak localization regime is measurably lower compared to a non-weakly localized environment.

Weak localization is broken by the application of a perpendicular magnetic field. By comparing the differences in conductance, values for l_e and l_ϕ based on a term l_B can be extracted. The application of a magnetic field breaks symmetry between time reversed paths. Clockwise and anti-clockwise paths experience phase differences due to the Aharonov-Bohm effect:

$$\Delta\phi = 4\pi\frac{BS}{\phi_0} \tag{A.5}$$

where B is the magnetic field, S is the area enclosed by the path, and ϕ_0 is the flux quantum, defined as h/e. The maximum path length that contributes to weak localization is right at the phase coherence length, $L \lesssim l_\phi$. The enclosed space is approximately:

$$S_{\max} \approx \pi(\frac{l_\phi}{2\pi})^2. \tag{A.6}$$

Suppression of weak localization starts at:

$$\Delta\phi \approx \frac{\pi}{2} = \frac{l_\phi^2}{2\phi_0}B_c \tag{A.7}$$

Leading to a critical magnetic field strength B_c of:

$$B_c \approx \frac{2\phi_0}{l_\phi} \tag{A.8}$$

$$l_c = \sqrt{\frac{\pi\phi_0}{B}} \tag{A.9}$$

Suppression starts when l_c approaches l_ϕ, and complete suppression occurs at $l_c \approx l_e$.

A.6 Future Work

More advanced devices were made on-chip, but unfortunately were not tested due to COVID-induced lab closures. These were double-AB ring devices, with two dispersive readout gates in hopes of measuring the interference two AB phases. This design closely mimics the topological layout of a Majorana-zero-mode device [274]. Dispersively sensing more novel AB designs with closer topological models to MZMs, such as fractional quantum Hall states [287] get us one step closer to a scalable MZM model.[1] Dispersive sensing of nanowires is proven to be effective [273], and recent advances in MZM devices [288] mean a dispersively sensed MZM is a realistic next step.

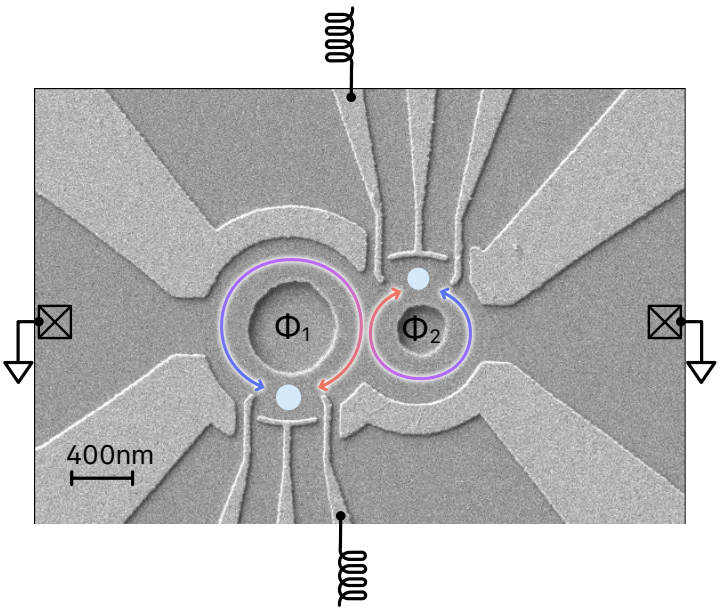

Figure A.4: **Next-generation AB design.** Schematic and micrograph of a double AB ring, featuring two dispersive sensing dots. This device is fabricated on the same GaAs chip as the first device presented in this work. Dispersive sensing gates are indicated by the inductors.

[1] The device in this citation features a large metallic island defining the inner ring boundary.

B

Additional Material for Spin Qubits with Scalable milli-kelvin CMOS Control

Many measurements not included in Chapter 5 are essential for a complete understanding of this work. Here, I detail methods and results that are particularly important to the device's performance. These measurements operate in the background to enhance overall stability and aid in the analysis of certain behaviors.

B.1 Fabrication

This device is based on a silicon metal-oxide-semiconductor (SiMOS) architecture, featuring two quantum dots and a single-electron transistor (SET). The gate structure sits on 800 ppm isotopically purified ^{28}Si, as natural silicon, containing approximately 4.7% ^{29}Si, contributes to fast dephasing of the electron spins. Palladium gates electrostatically define the quantum dots and SET via a multi-gate stack technology. The gates are electrically isolated via aluminum oxide atomic layer deposition (ALD), and a thermally grown SiO_2 layer on the silicon surface reduces gate leakage to the bulk substrate.

The device contains two ohmics and 14 gates. These serve as the SET (ST, SRB, SLB), SET barrier to the dots ($SETB$), plunger gates defining the quantum dots and dictating electron occupancy ($P1$, $P2$), tunnel coupling modulation (J), reservoir barrier gates (B, $P3$, $ResB$), a reservoir accumulation transport gate (Res), two side-barrier gates (LB, RB), and the microwave antenna. This device is designed to form three dots, but due to leakage characteristics of $P3$, only

two dots could be formed.

B.2 Temperature Control

The majority of this experiment is performed at a fridge base temperature of 20 mK with ^{3}He circulation. A mixing chamber stage heater is activated for experiments requiring raised temperatures between 20 mK and 700 mK. The ^{3}He mixture is partially removed to target temperatures between 700 mK and 1.4 K (see Fig. B.12). For higher temperature measurements (3.5 K), not included here, the ^{3}He mixture is completely removed and the system relies solely on pumping on the 1 K pot.

B.3 Pulse Shaping for AC-Coupled Gates

The qubits, resonator, and cryo-CMOS are mounted on a custom PCB with on-chip bias tees for integrating DC signals and high-frequency pulses. The gates on the qubit chip have three different kinds of connections: DC-only, DC and high frequency, and cryo-CMOS, indicated in Fig. B.1 (a). Most gates require only DC voltages, as they serve as barriers for finely tuning the SET and quantum wells for appropriate electron occupation. Two gates (J and B) are connected to cryo-CMOS, and when operating in pass-through mode the DC and baseband signals are combined via a high-bandwidth combiner at room temperature. The three remaining gates requiring high frequency pulsing but are not connected to cryo-CMOS ($P1$, $P2$, ST-SET) use the PCB bias tees for signal combination. The high frequency components are AC-coupled, requiring careful pulse shaping to replicate longer square pulses.

The decay rate of the AC signal is measured in Fig. B.1 (b) using the SET current to determine the settling time required after pulsing. State preparation and measurement most commonly require pulsing of $P1$ and $P2$ (for detuning); therefore without an opposite compensating pulse a settling time of approximately 5 ms is required. While this is well within the margin of T_1, it significantly slows total measurement time. The execution of longer measurements, such as randomized benchmarking, becomes problematic due to the increased probability of instrument failure due, dropped communication links, and other bugs. Many measurements in feature an opposite polarity compensating pulse to shorten this settling time.

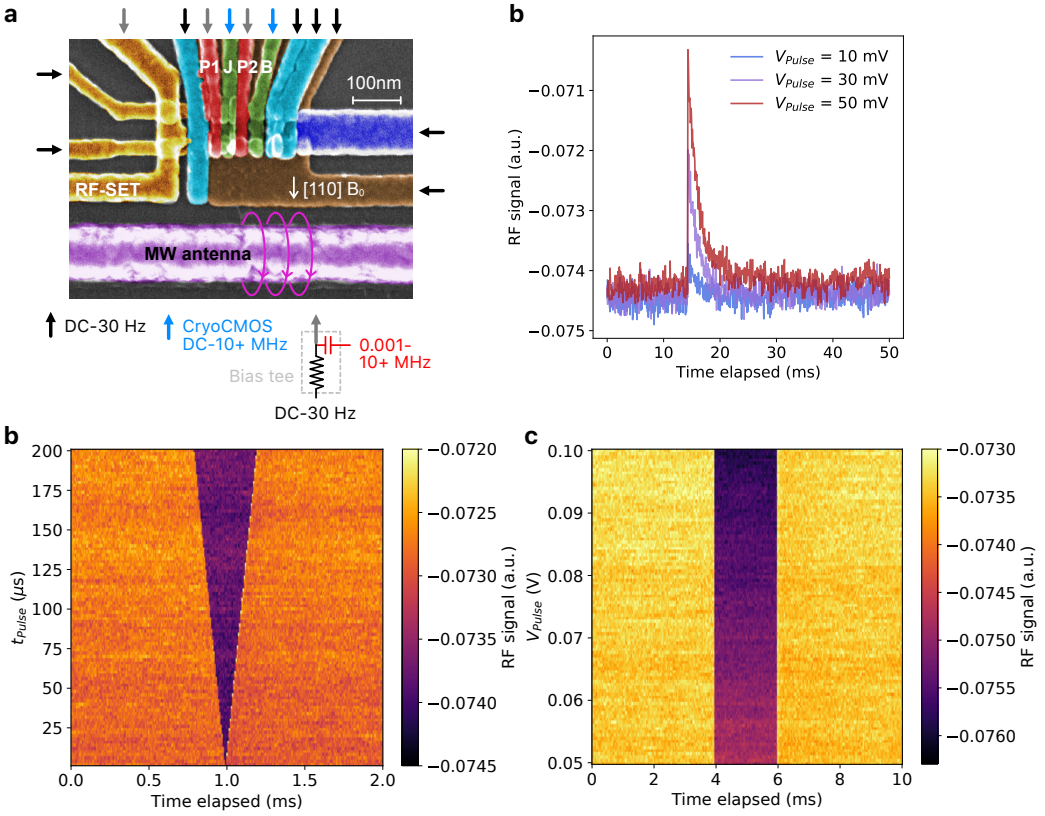

Figure B.1: **Gate connections and pulse shaping for decay compensation. a,** Micrograph of the device tested and indicators of the type of connection to each gate. Most gates require DC-only sources, and those controlled by cryo-CMOS are DC-coupled. There are three gates, $P1$, $P2$, and ST (comprising part of the SET) connected to AC-coupled pulse lines. The key below the image indicates the approximate frequency range covered by the DC- and AC-coupled lines. **b,** Decay of an AC pulse with respect to the pulse amplitude, measured by the SET response. All pulses decay exponentially, with larger pulses requiring a longer settling time to return. **c-d,** Through precise pulse engineering, AC-coupled lines are capable of producing square pulses with a wide range of pulse times (c) and amplitudes (d) that encompass all pulsing requirements of this experiment.

B.4 Coulomb Diamonds

Coulomb diamonds are measured by passing current through the device to calculate the lever arm and charging energy of the quantum dots. The regular pattern in Fig. B.2 indicates acceptable dot formation and the need for little bias offset. These diamonds are not used directly in the analysis of other results, rather they serve as a sanity check for both the evolution of dot occupation and electron temperature measurements that use lever arm calculations. Unlike all other measurements presented in the main body chapter, these use DC transport for readout.

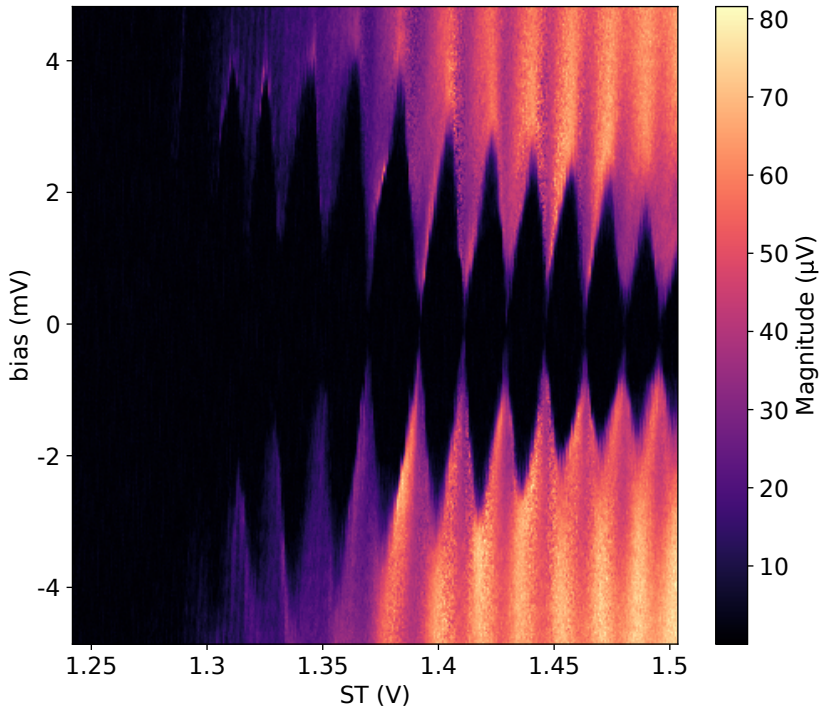

Figure B.2: **Coulomb diamonds measured through the device.**

B.5 State Preparation and Measurement

The Diraq Si qubit devices include a reservoir to populate the quantum dots. This device can operate in both a reservoir and an 'isolated' mode, where the dots are isolated from the reservoir. Numerous early device evaluations are completed in reservoir mode, establishing baseline results for double dot tuning, SET performance, and the presence of Pauli spin blockade. For better control using cryo-CMOS, single- and two-qubit measurements are conducted in an isolated mode configuration. Tunnel barrier modulation (principally by gate J) requires more complex pulsing involving $P1$ and $P2$ in a reservoir mode compared to isolated mode, where only the J-gate is used for modulation.

In order to isolate the quantum dots, electrons first must be loaded from a reservoir and measured to determine occupation. While plunger gate ($P1$, $P2$) tuning is similar between the two modes, isolation can be tricky, as raising the barrier often unexpectedly ejects some electrons. The loss or gain of an electron requires a complete re-initialization of the dots.

Fig. B.3 (a) shows a typical double dot stability diagram with indicated dot occupations. By isolating the dots from the reservoir (Fig. B.3 (b)), only the inter-dot transitions remain. Isolation

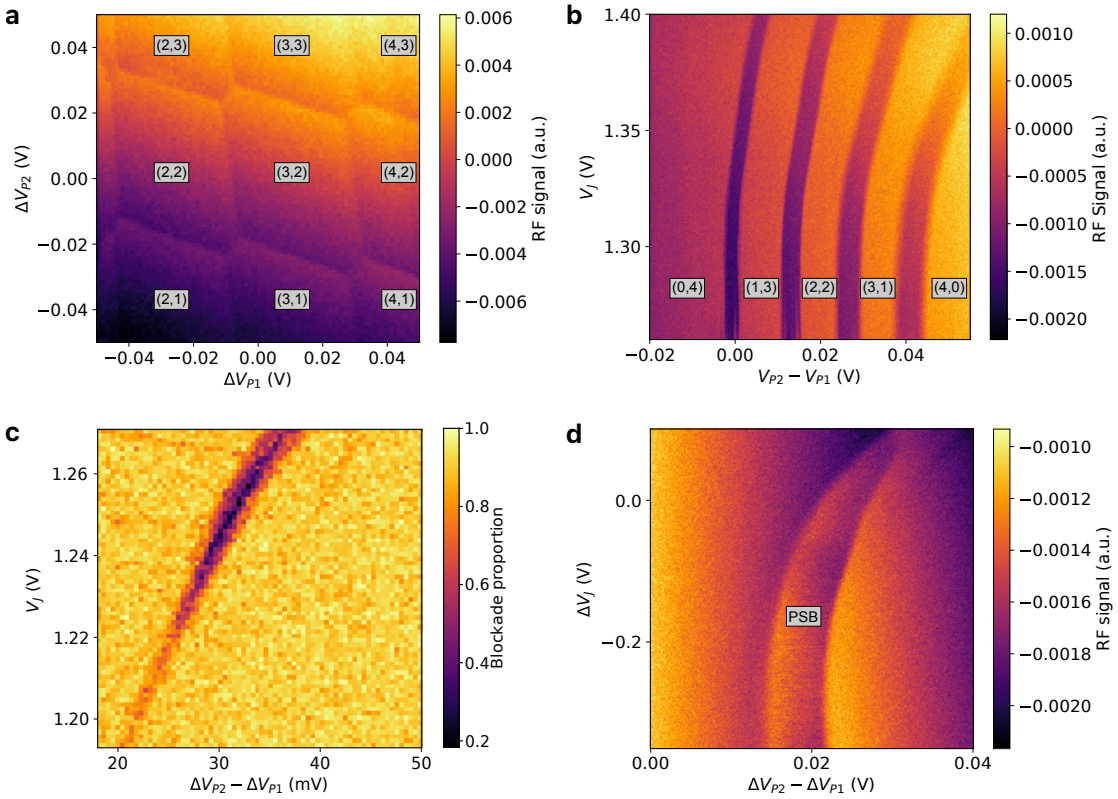

Figure B.3: **Electron configuration and critical SPAM windows. a**, Charge stability diagram when varying the plunger gates $P1$ and $P2$. Electron occupancies of the two dots are indicated. **b**, By isolating the dots from the reservoir, only inter-dot transitions are seen. These transitions are a function of detuning and inter-dot coupling, modulated by the J-gate. The increasing line width is due to the measurement technique that improves transition visibility. **c**, T^- initialisation window as a function of detuning and tunnel coupling. This zone sits close to the inter-dot transition and disappears at both higher and lower V_J. **d**, Pauli spin blockade window between the (0,4) and (1,3) transition, as a function of detuning and tunnel coupling. At higher V_J the window closes, and at lower V_J (outside the data presented) the tunneling rate drops below that of the measurement time, leading to unusual features that are readout-frequency dependent.

allows for the easy addition of a third parameter–inter-dot coupling–that is measured as a function of detuning ϵ ($P1 - P2$). The slight bend in the transition lines is due to the misalignment of gates during fabrication, breaking the symmetry between $P1$, J, and $P2$. This particular configuration of four total electrons was incredibly stable, remaining in this charge state for months before an event (my user error) changed electron occupation.

Two specific preparation states are used throughout this experiment: mixed and T^- initialization. A comprehensive overview of these two states and their use case is in chapter 3. Qubits

are initialized into their spin states by transferring an electron over such that the dot occupation is (0,4). Waiting for relaxation for initialization is impractical due to the long T_1 decay rates, and in this isolated mode, new electrons can't be exchanged from the reservoir such as in [289]. Instead, the electron is quickly relaxed to the ground state in a 'hot-spot'[1] region in the (0,4) occupation, facilitating initialization times of $500\ \mu$s. T^- initialization takes on an extra step, relaxing into the $|\downarrow\downarrow\rangle$ state in a narrow region shown in Fig. B.3 (c). Here a line shows where optimal T^- initialization is achieved via relaxation. A slow drift across the feature gaining the most pure results. The T^- initialization window in V_J is finite, and it is fortunate that this window overlaps with the further overlap of exchange and readout windows when using cryo-CMOS control. The dot occupation is shuffled back to the (1,3) charge configuration for further operations.

Under a magnetic field, a Pauli spin blockade window opens in the (0,4)-(1,3) transition, as seen in Fig. B.3 (d). This window is quite wide, allowing for straightforward tuning for spin-blockaded readout. At higher V_J, the window begins to close, and the blockade itself becomes inconsistent, likely due to induced spin-flipping when shuttling electrons.

B.6 Rabi Tuning

The frequency of Rabi oscillations is proportional to the power applied at the microwave gate. Maximizing the fidelity of single- and two-qubit gates requires Rabi frequencies as fast as practically possible. In this experiment, a maximum Rabi frequency of 1 MHz is achieved before saturation and degradation of the gate fidelity occur. This drop in fidelity at higher frequencies is attributed to excessive heating from the microwave line.

[1] These are regions of especially fast decoherence.

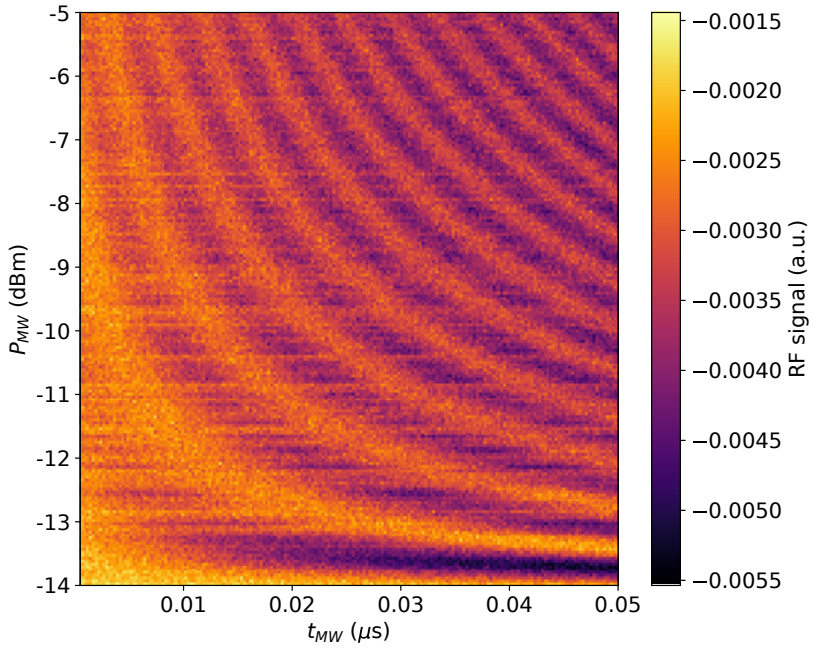

Figure B.4: **Increasing Rabi oscillation frequency as a function of microwave power.**

B.7 Feedback Protocols

Fluctuations in the local and broader environment cause device drifting, necessitating the implementation of certain feedback mechanisms. Each feedback protocol incurs a computational and time overhead, so their implementation depends on the extent to which drift affects the measurements. All protocols detailed here were implemented during the experiment. Feedback strategies are chosen proportionally, as more sophisticated PID loops do not justify the (marginally) increased accuracy compared to their computational overhead.

B.7.1 SET Feedback

The most critical feedback protocol is SET feedback. Movement of an electron between quantum dots shifts the SET Coulomb blockade. By actively measuring the signal at the side of a Coulomb peak, any shift in the peak causes a significant change in signal, acting as a sensitive charge sensor. Once the signal difference is measured, the Coulomb peak must be returned to its original position; otherwise, there is a risk of losing the measurement sensitivity as it drifts away. Feedback is performed at the end of every measurement. An alternative method explored but not implemented involves constant SET feedback on a separate thread, independent of ongoing operations. This approach offers benefits such as reduced overhead but is prone to errors when retuning the device.

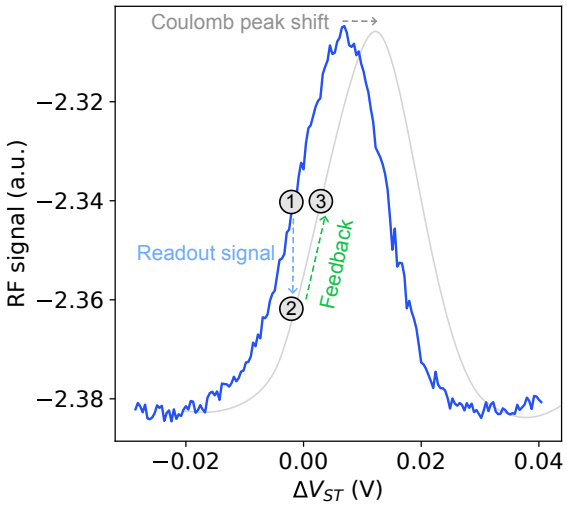

Figure B.5: **SET feedback.** A change in charge occupancy results in the shift of a Coulomb peak in the SET. Sitting on the side of the Coulomb peak results in the most sensitive signal readout (1 → 2). Once the signal has been measured, the readout point is returned to that same position on the peak via proportional feedback (2 → 3).

B.7.2 Detuning Feedback

Initialization and readout require precise voltage control in detuning ϵ. Drift in detuning due to charge noise and other mechanisms significantly impacts measurements. This feedback protocol is implemented in experiments requiring T^- initialization as drift impacts the purity of the initialization.

Detuning feedback tracks changes in the (0,4)-(1,3) transition and corrects all voltage points for slight drifts relative to the crossing. The amount of drift is determined by sweeping over the transition and analysing the integrated SET current. Proportional adjustments are made based on changes to the initial measured value. Without this feedback enabled, drift is on the order of millivolts per minute. Detuning never drifted further than 1 mV, not of concern for most situations as the Pauli spin blockade window (Fig. B.5 (d)) is ten times larger, not to mention the comparatively enormous mixed initialisation windows.

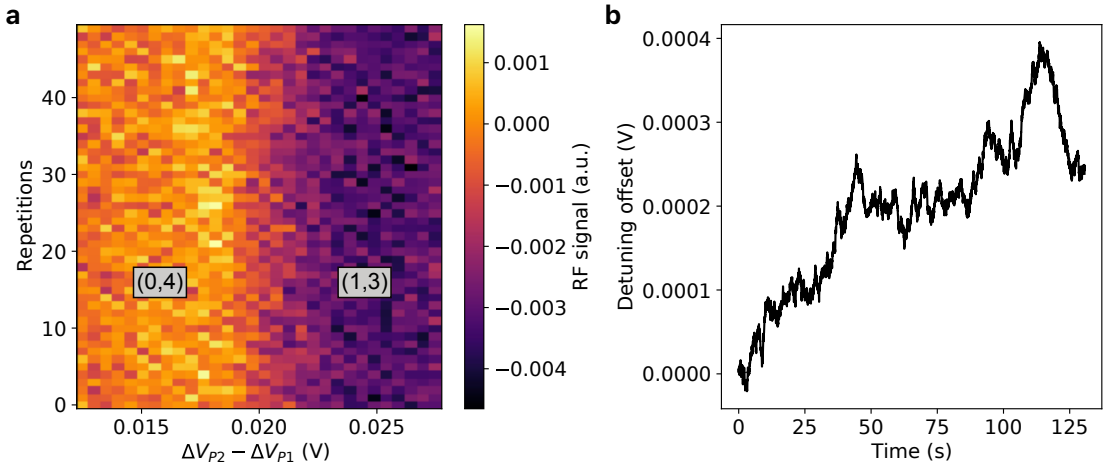

Figure B.6: **Detuning feedback. a,** Actively corrected (0,4) $\rightarrow$ (1,3) transition using detuning feedback over 50 repetitions. Without feedback in place, the transition variation is visible by the user. **b,** Voltage offset required for constant detuning voltage placement over the course of the measurement. There are many more points than 50 repetitions here, as each point instead correlates to one measurement (500 points, 10 averages per line in a). The offset value is used for gate $P2$, and the negative for $P1$.

B.7.3 Frequency Feedback

For direct quantum gate feedback methods, frequency feedback ranks first in importance due to its outsized impact on device performance. Shifts in qubit frequencies over 200 kHz lead to completely incoherent qubit operations if feedback is not implemented. Further, the drifting behavior

of both qubits is different, with qubit two's (Q2) drift far more dramatic and chaotic than qubit one (Q1). Fortunately, the overhead for this feedback is minimal, requiring only one extra sequence per qubit per measurement.

This feedback protocol adjusts for shifts in the Larmor frequency using a modified Ramsey sequence. A $\sqrt{X}$ gate is applied to the pure state target qubit, where it is left to freely precess over a set period of time (typically 10π rotations). After, the qubit is projected onto the $\pm y$ axis through a $\pm\sqrt{Y}$ gate. Ideally, these two projections should yield equal spin flip probabilities. If not, a proportional adjustment in the qubit frequency is made before further qubit operations.

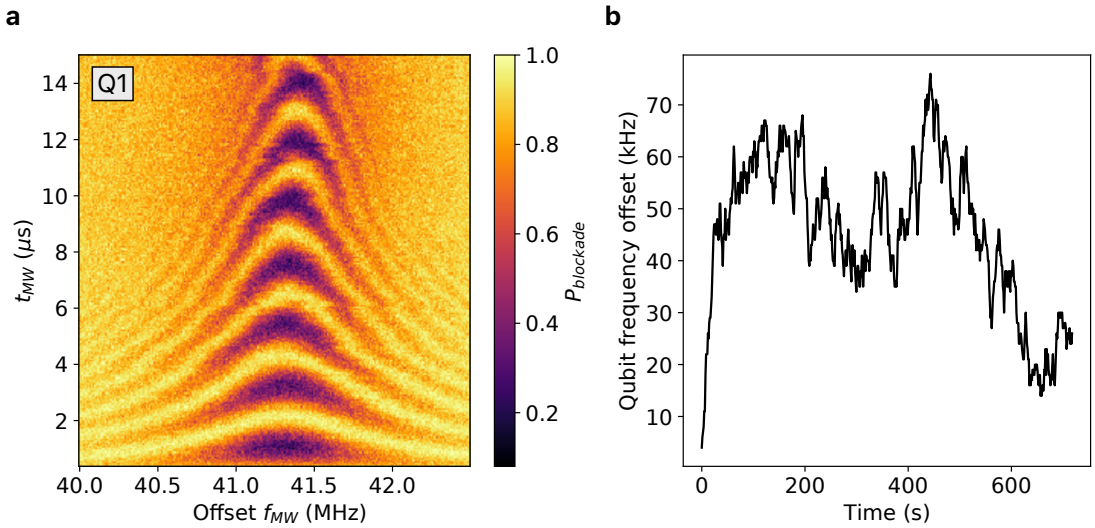

Figure B.7: **Frequency feedback. a,** Rabi chevron of Q1 with frequency feedback disabled. Compared to other Rabi chevrons presented in my thesis, this shows significant drift over time as longer t_{MW} times are explored. **b,** Frequency offset correction from the original measured resonant frequency of the qubit. Over approximately 12 minutes, the qubit resonant frequency shifts by over 70 kHz.

B.7.4 Rabi Feedback

The Rabi frequencies of qubits are also susceptible to drift, influenced by the local environment and changes in room temperature. Over several hours, the Rabi frequency can shift in proportion to the lab temperature, affected by the varying output power of the microwave source. Shifts by up to 3% have been observed, however unlike frequency and detuning, the shifting rate is far slower, encompassing hours rather than minutes. The relatively minor short-term impact allows for less frequent adjustments, reducing overhead. For instance, while SET and frequency feedback are implemented for every shot, Rabi feedback can be measured every n^{th} run, typically once per aver-

aged data point. This greatly reduces measurement time while retaining the bulk of the feedback effectiveness. Fig. B.8 (b) shows the adjustment of the microwave amplitude over a 10 hour period, demonstrating the stability of the qubit over this time frame. Rabi feedback is only effective when combined with frequency feedback.

A $\pi/2$ pulse time for the target qubit is established by measuring a frequency feedback-enabled Rabi chevron and fitting to the resonant frequency. Seven and nine $\sqrt{X}$ gates are applied to the target qubit. Ideally, without feedback, the spin proportion of these gates should be identical (0.5). Any adjustments due to under- or over-rotation are applied to the IQ input power to the microwave source.

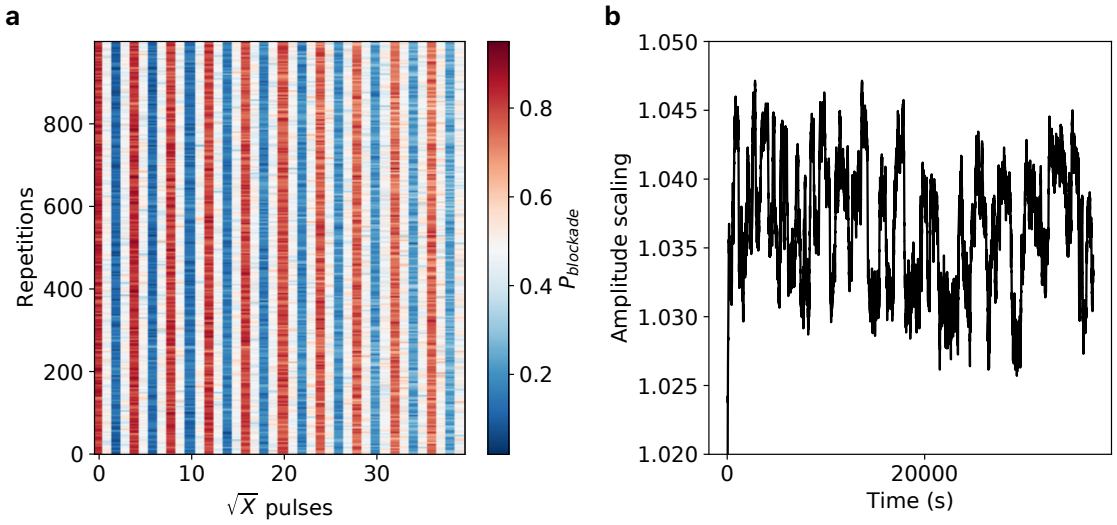

Figure B.8: **Rabi feedback. a,** Simple sequence to test Rabi feedback. Successive $\sqrt{X}$ are applied to the target qubit, and the sequence is repeated over a period of time. The blockade of the spin is dependent on the number of pulses, assuming that the Rabi frequency is correct. This sequence allows for the adjustment of Rabi frequency over a long period of time to understand the expected drift magnitude as well as speed at which the Rabi frequency changes. **b,** Microwave amplitude scaling correction for Rabi frequency adjustment of the qubit. The amplitude almost immediately shifts 4% before correcting for small adjustments over a period of 10 hours.

B.7.5 Exchange Feedback

Finally, the most complex feedback protocol implemented is exchange feedback. Even a small change in voltage applied to the J-gate can cause significant variation in the exchange rate between two qubits. Consistent two-qubit interactions necessitate a stable exchange, requiring precise adjustments to the J-gate pulse amplitudes.

The implementation of this protocol is complex as it involved interaction with the cryo-CMOS. Using RT control only, it's a relatively simple direct adjustment of the J-gate amplitude. This is not possible under cryo-CMOS control, instead we adjust V_{HIGH} and V_{LOW}, voltage inputs directly into the cryo-CMOS that determine the J-gate pulse amplitude. This results in noticeable heating as these input lines are not intended for fast pulses and requires significant calibration due to complex interactions between V_{HIGH}, V_{LOW}, and V_J (see section B.11 for more details). Furthermore, if every single J-gate in a multi-qubit system requires adjustment, this kind of implementation defeats the purpose of this experiment, as we would never achieve any real reduction in RT-20 mK connections. Correcting J-gate pulse time is another option, however it is less accurate, limited by the clock resolution of the FPGA (4 ns).

The traditional feedback approach involves initializing the target qubit along the y-axis and the control qubit on the z-axis. The J-gate is pulsed for time t to perform a CZ gate several times (typically 5) followed by a $\pm\sqrt{Y}$ gate on the target qubit to project the spins back onto the $\pm z$-axis. As with Rabi feedback, the ideal spin proportions are 0.5, and any mismatches are adjusted accordingly. A DCZ version of this protocol requires minimal modification.

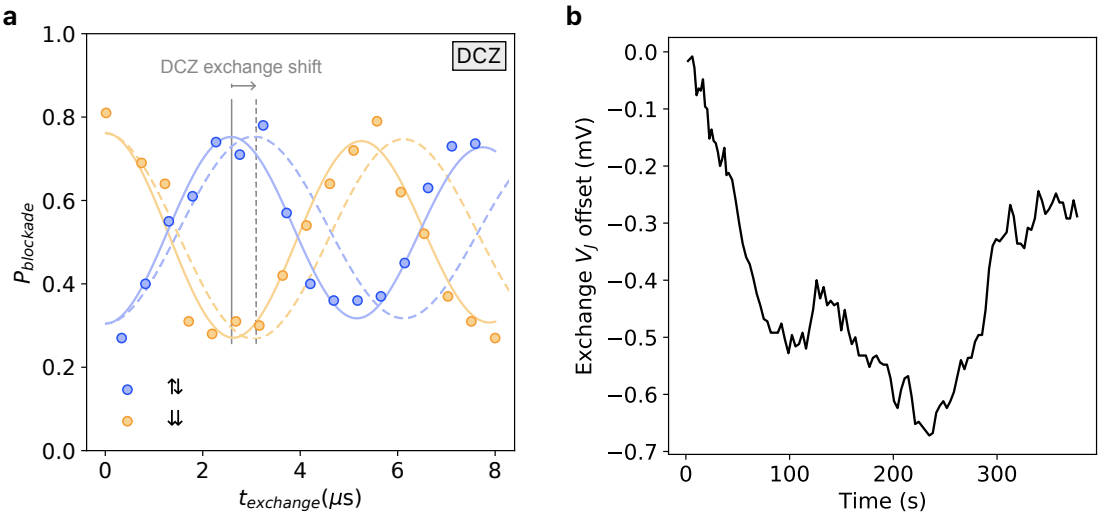

Figure B.9: **Exchange feedback. a,** Schematic illustrating the possible shift of DCZ oscillations. A single DCZ gate is denoted by the solid and dashed vertical lines. A lower exchange rate results in longer exchange time, requiring adjustment of the J-gate pulse amplitude to compensate. As illustrated here, a lengthening of the exchange time with no compensation results in under-rotation, reduced fidelity and reduced visibility. **b,** J-gate amplitude scaling to compensate for shifts in exchange. Maximum deviations observed were 1 mV away from the set value, but these represent extreme circumstances and typical corrections are on the order of microvolts.

Some device drift is attributed to the presence of ^{29}Si impurities in the ^{28}Si substrate. Reducing

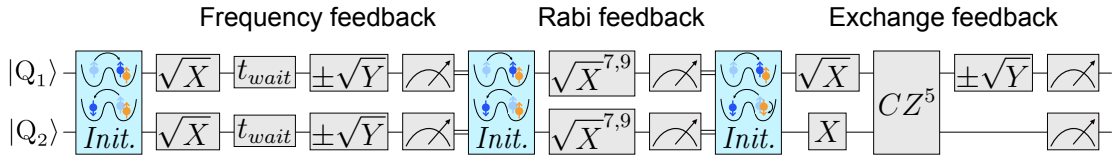

Figure B.10: **Feedback circuits.** Schematic of an example quantum circuit utilizing feedback protocols (detuning and SET feedback not shown). In many experiments, feedback protocols were implemented in this way, often repeated a number of times before execution of the experiment itself. Each sub-circuit requires re-initialisation due to quantum state collapse after readout and feedback. This circuit order ensures proper calibration, as (for example) exchange feedback may not work properly without frequency and Rabi feedback respectively.

the impurity count improves device stability and reduces the need for frequent feedback. This has been shown recently with devices featuring a 50 ppm impurity count [290], and industrial fabrication processes are likely to reduce defects and impurities even further [291–293]. Recently, a new study has reported the reduction of ^{29}Si down to 2 ppm [294]. Consequently, future devices are likely to be ultra-stable, significantly diminishing the need for current feedback protocols and greatly enhancing their capabilities as feedback overhead becomes negligible.

B.8 Further Details on Qubit 2 Performance

The behavior of Q1 and Q2 is different throughout the experiment, in general with Q2 exhibiting worse outcomes. Aside from the presence of a Stark shift, Q2 has poorer T_2^* and T_2^H coherence times (Fig. 5.8) and lower fidelities (Fig. B.11). Additionally, Q2 experiences greater and more erratic resonant and Rabi frequency drift compared to Q1. In two-qubit measurements, Q2 is exclusively used as the control qubit to minimize its impact on the system. The exact cause of this behavior is unclear, but it is likely due to asymmetries in device fabrication and the presence of proximal ^{29}Si atoms (or other impurities) contributing to decoherence.

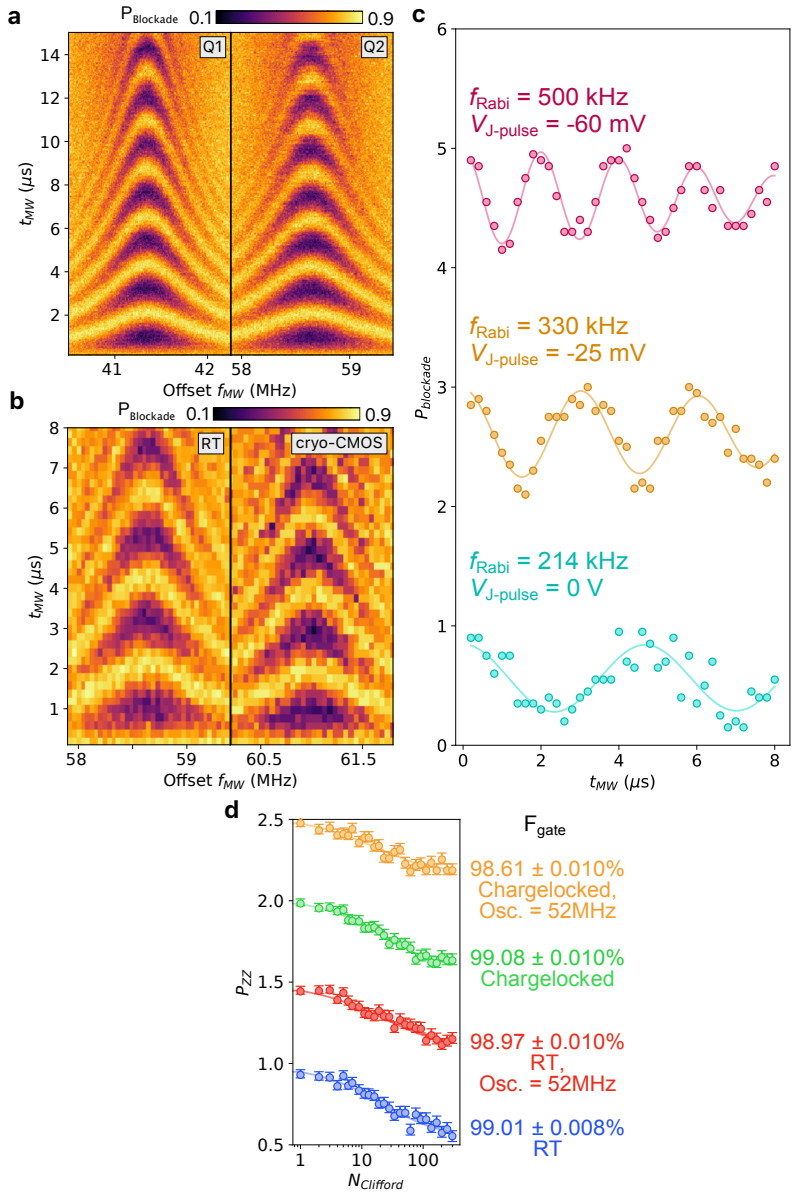

Figure B.11: **Extra Q2 behavior data. a,** RT Rabi chevron comparison between Q1 and Q2. When well optimized, Rabi frequency and visibility of the two qubits are similar. **b,** Q2 RT and cryo-CMOS Rabi chevrom comparison. Under both control conditions with identical voltage-pulsing, Rabi oscillations are near-identical. **c,** Q2 exhibits unusual shifting Rabi frequency with tunnel coupling. Rabi frequency increases as as tunnel coupling is lowered, demonstrated by the different J-gate pulses that modulate the tunnel barrier. **d,** RBM fidelities of Q2, under the same conditions reported in Fig. 5.2 (b). Q2 generally had lower coherence and therefore fidelities in comparison to Q1.

B.9 Randomized Benchmarking

In this experiment, single qubit randomized benchmarking (RBM) sequences are constructed from $\pm X/2$, $\pm Y/2$, $\pm Z/2$, $\pm X$, $\pm Y$, $\pm Z$ and I gates. Similarly, two-qubit RBM (2QRBM) is composed of the same gates for both qubits as well as a DCZ gate. General details of randomized benchmarking can be found in section 3.3.3. After fitting to equation 3.35, a single qubit Clifford fidelity is extracted using $1 - 0.5b$, and two-qubit fidelity form $1 - 0.75b$ [295].

2QRBM was attempted in this experiment, however the results were not conclusive enough to present. Both intrinsic device behavior and cryo-CMOS limitations prevented the extraction of an accurate gate fidelity. Two qubit Clifford gate length constituted a significant fraction of T_2^*, which lead to low visibility, excessively long measurement times and data fitting with fidelity error values exceeding 10%. The minimum single-qubit gate time (approximately 500 ns) was slow and could not be pushed higher as this lead to a decrease in single qubit fidelity. The two-level restriction due to cryo-CMOS control meant that two qubit gates also were too long, and readout visibility constantly diminished with decreasing gate time.

B.10 Thermal Observations

In future experiments, better thermal design is required, and some of the suggestions are found in section 6.3. Absent of these changes, the electron temperature scales linearly with mixing chamber temperature, however at a much higher rate. Fig. B.12 presents additional data to Fig. 5.2 (d), adding in the measured electron temperature.

B.11 "Why can't you just pulse on the input voltage lines?"

One of the primary limiting factors of this cryo-CMOS design is the restriction to only two voltage levels. This meant that especially for two-qubit gates I was effectively calibrating with one hand tied behind my back. I've detailed future improvements to cryo-CMOS devices in Section 6.3, but for our current device we had to try and find other methods of getting around this problem. An idea broached by the team was pulsing on the input lines V_{HIGH} and V_{LOW}. Naively, this approach is sound, as we were pulsing on V_{HOLD} when under room temperature control, such that the cryo-CMOS was acting like a transparent block. So, by precisely pulsing one of these lines under cryo-CMOS control, we have access to a third (or even fourth) voltage level, lifting this limitation. During a DCZ operation, for example, the two default levels are chosen to maximize single qubit

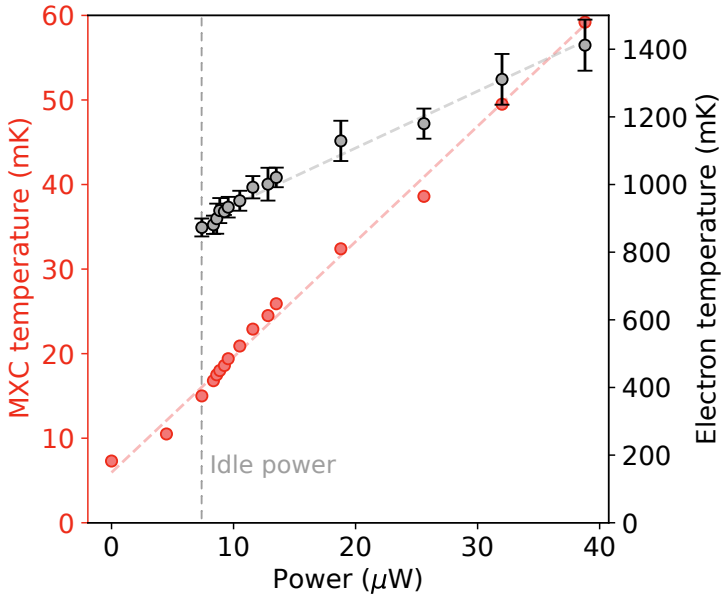

Figure B.12: **Mixing chamber and electron temperature correlations.** Mixing chamber temperature and electron temperature scale linearly with power consumption, but due to poor thermalization the electron temperature rises at a much faster rate.

control speed and readout visibility. V_{HIGH} and V_{LOW} are pulsed during stages of state preparation and exchange to optimal J-gate voltage levels. Due to the complex interaction between V_{HIGH} and V_{LOW}, we require pulses on both gates for calibration purposes. Pulse amplitudes are on the order of 100 mV.

In practice, we found that this pulsing technique lead to a significant increase in the mixing chamber temperature, up to hundreds of milli-kelvin and well beyond what was observed with the activation of the oscillator. Comparing mixing chamber temperature to electron temperature in Fig. B.12 and extrapolating, the possible electron temperature when pulsing is too high for effective qubit operation. This result, while unusual, should not be surprising given that this cryo-CMOS chip is not designed to accept fast square pulses on these lines. Electrostatic discharge diodes or other on-chip components are likely contributing to the heat generation observed.

B.12 Concluding Remarks

This experiment in totality took two years, from initial idea, PCB design, fridge setup to device testing and analysis of final results. Housed in a Bluefors LD-400, in total 24 additional SMA and 50 additional DC lines were installed and several (mostly superconducting readout lines) were

replaced after hours of debugging. Eight Si devices and two cryo-CMOS chips were tested, and only one of each constitutes all the results presented here. It was an enormous task, requiring me to learn about spin qubit physics, control techniques, and some basic cryo-CMOS ASIC design and was the final project of my PhD. This was by far my favourite experiment, and one I hope to expand on in some capacity in the future.

C

Time-Division Multiplexing of Semiconductor Qubits

Not all experiments succeed. At the outset of my thesis, I continued the work of a previous student, M. C. Jarratt, on a time-division multiplexing protocol. As briefly mentioned in the conclusion (chapter 6), time-division multiplexing will be crucial for scaling up quantum systems. However, several factors prevented its realization here and subsequent publication of this experiment.

Current strategies for quantum state readout consume significant resources, making it inefficient to duplicate these systems. Sharing resources among many qubits is crucial for scalability. A design incorporating time-division multiplexing (TDM), which enables efficient readout of multiple quantum systems, is partially realized on a GaAs quantum dot device equipped with several quantum point contact charge sensors. This device features lithographically defined switches that do not impact the impedance matching network. Using fast RF readout techniques allows for the measurement of multiple quantum dots using the same readout circuit, within reasonable T_1 lifetimes of spin qubits.

C.1 Introduction

Readout networks comprising charge sensors, microwave components and corresponding circuitry constipate some of the largest and most resource-intense aspects of quantum systems. Current strategies often duplicate the entire readout network as the number of qubits scale, which is a highly inefficient approach. At high qubit numbers, space constraints and cooling power inside cryogenic

systems deems this brute force approach infeasible. Consequently, sharing these resources among multiple qubits is essential for scalable readout technologies.

Many advances in efficient readout have been made in the frequency domain [9, 296]. While frequency multiplexing offers a partial solution, certain limitations prevent it from being a comprehensive solution for readout scalability. These limitations include frequency crowding and space constraints, as the number of impedance matching networks scales with the number of charge sensors. Additionally, the need for extra gate paths, ohmic contacts, and/or multiplexing chips reduces the available space on a quantum device and increases the requirements for room temperature instrumentation. A new methodology utilizing time-domain multiplexing promises to reduce these instrumentation needs and minimize the real estate occupied by quantum device readout technologies.

Time-division multiplexing (TDM) is a method in which the quantum state of qubits is read sequentially. A single readout circuit and impedance matching network can be connected to multiple charge sensors, allowing for the readout of a large number of qubits, provided that individual readout times are significantly shorter than the T_1 lifetime of the qubits. Achieving this requires the use of fast switches to individually connect the readout chain to each charge sensor in sequence. Instead of using multiple frequency channels simultaneously for readout, only a single frequency channel common to all charge sensors is needed. The schematic for such a circuit is shown in Fig. C.1.

The switch used in this setup has specific requirements that cannot be fulfilled by off-the-shelf components. It must be small, fast, low power, and have a low switch capacitance C_{switch} to minimize the load on the impedance matching network. Traditional MOSFET switches fail to meet all these criteria, as their typically higher switch capacitance of approximately 3 pF [297] reduces the switching frequency due to longer charging times ($t = RC$), and results in significant power dissipation at high frequencies. The power dissipated by a switch is given by:

$$P = \frac{1}{2} C V^2 f \tag{C.1}$$

where C is the capacitance, V is the voltage switching amplitude and f is the frequency. At a 100 MHz switching frequency, the heat generated by *one* switch is similar to the cooling power of cryogenic refrigerators at base temperature (10 mK, 20 μW). Power dissipation must be orders of magnitude lower in order for this scheme to be viable at high qubit numbers.

Instead, an on-chip switching platform is used. These switches meet all the necessary requirements: they are micron-sized and have low switch capacitance, enabling nanosecond switching speeds and low power dissipation [2, 298]. In this design, multiple paths are defined on a two-

dimensional electron gas (2DEG), each connecting an individual charge sensor to a single impedance matching network, and can be switched using voltage pulses on gate electrodes.

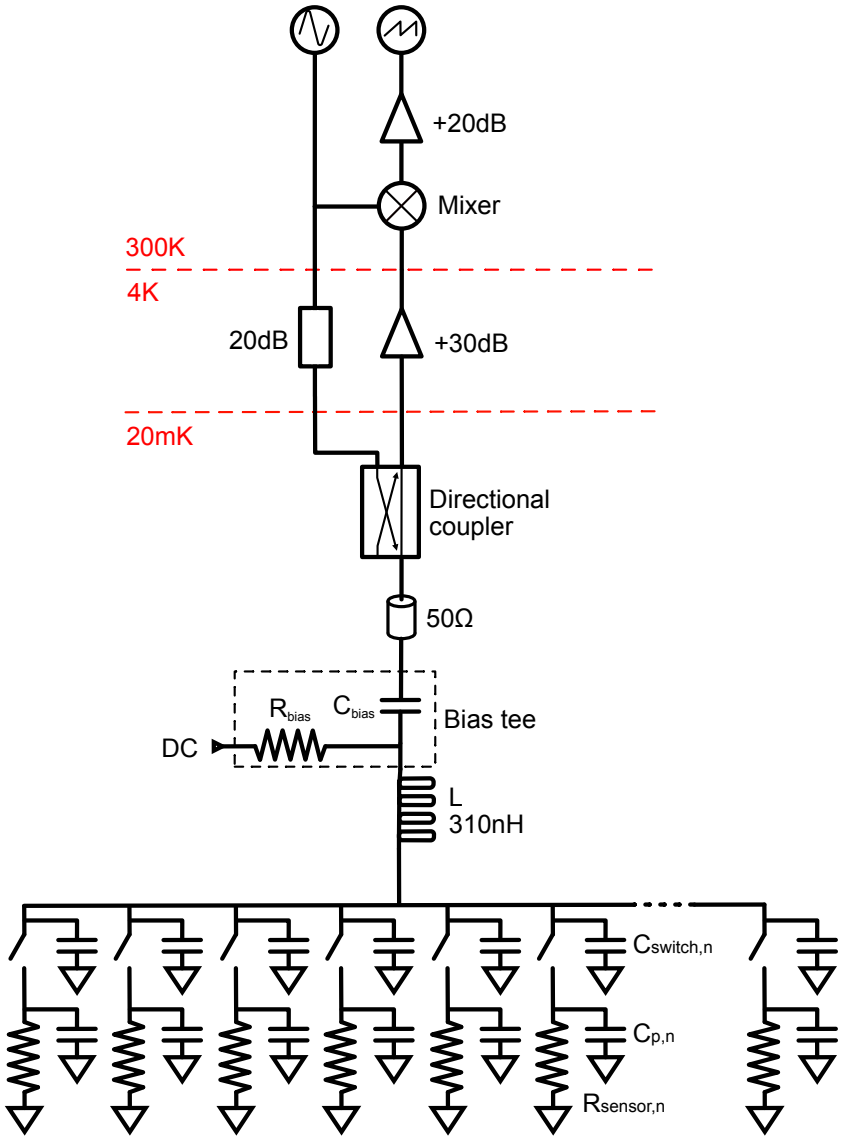

Figure C.1: **Time division multiplexing schematic.** Schematic of a time-division multiplexing switch matrix. Multiple devices are connected to a single RF readout channel via a number of switches. Each switch as a corresponding capacitance C_{switch}, and each device a corresponding resistance and parasitic capacitance.

C.2 Experimental Setup

The on-chip switch is implemented in conjunction with a double quantum dot design, as shown in Fig. C.2. This devices is based on a GaAs/$Al_{0.3}Ga_{0.7}As$ 2DEG, with the 2DEG heterostructure junction 91 nm below the surface. Gate electrodes are patterned on the surface to electrostatically define regions of the 2DEG, and a 10 nm layer of Al_2O_3, deposited using atomic layer deposition, separates the surface of the GaAs chip from the TiAu gates, preventing electron tunneling between these gates and the 2DEG underneath. The 2DEG is electrically connected using annealed ohmic contacts, see appendices D and E for details on their fabrication. Three annealed ohmic contacts, one source, and two drain reservoirs (for two charge sensors) are used for operation. These are used in the conventional manner, serving as DC transport reservoirs or, in the case of the drains, as capacitively coupled RF grounds.

For RF measurements, the single source ohmic is wire-bonded to an impedance-matching network with a parasitic capacitance of approximately 0.2 pF. This impedance matching network comprises an LC resonator, consisting of a superconducting spiral NbTi 310 nH inductor and capacitor. The resonator is one of eight on chip resonators developed for frequency multiplexing techniques [9]. A 40 nm AuPd resistive layer and 40 nm NbTi plate together form a bias tee, allowing for DC voltages to be applied to the source ohmic.

The device and resonator are mounted on the same PCB board at the mixing chamber of a dilution refrigerator. The fridge has a base temperature of 15 mK, and reflected RF signals are amplified at the 4 K stage before passing through a demodulation circuit discussed in section 2.4. The circuit diagram for this setup is similar to Fig. C.1, however with only two switches present. Both DC and RF readout are possible with this setup; however, for the speed of operation and demonstration of on-chip switch characteristics, we primarily opt for RF readout. Gates L, LP, C, RP, R, and T_f define the double quantum dots. Quantum point contacts for readout are formed between gates $QPC1$ and L, and $QPC2$ and R, respectively.

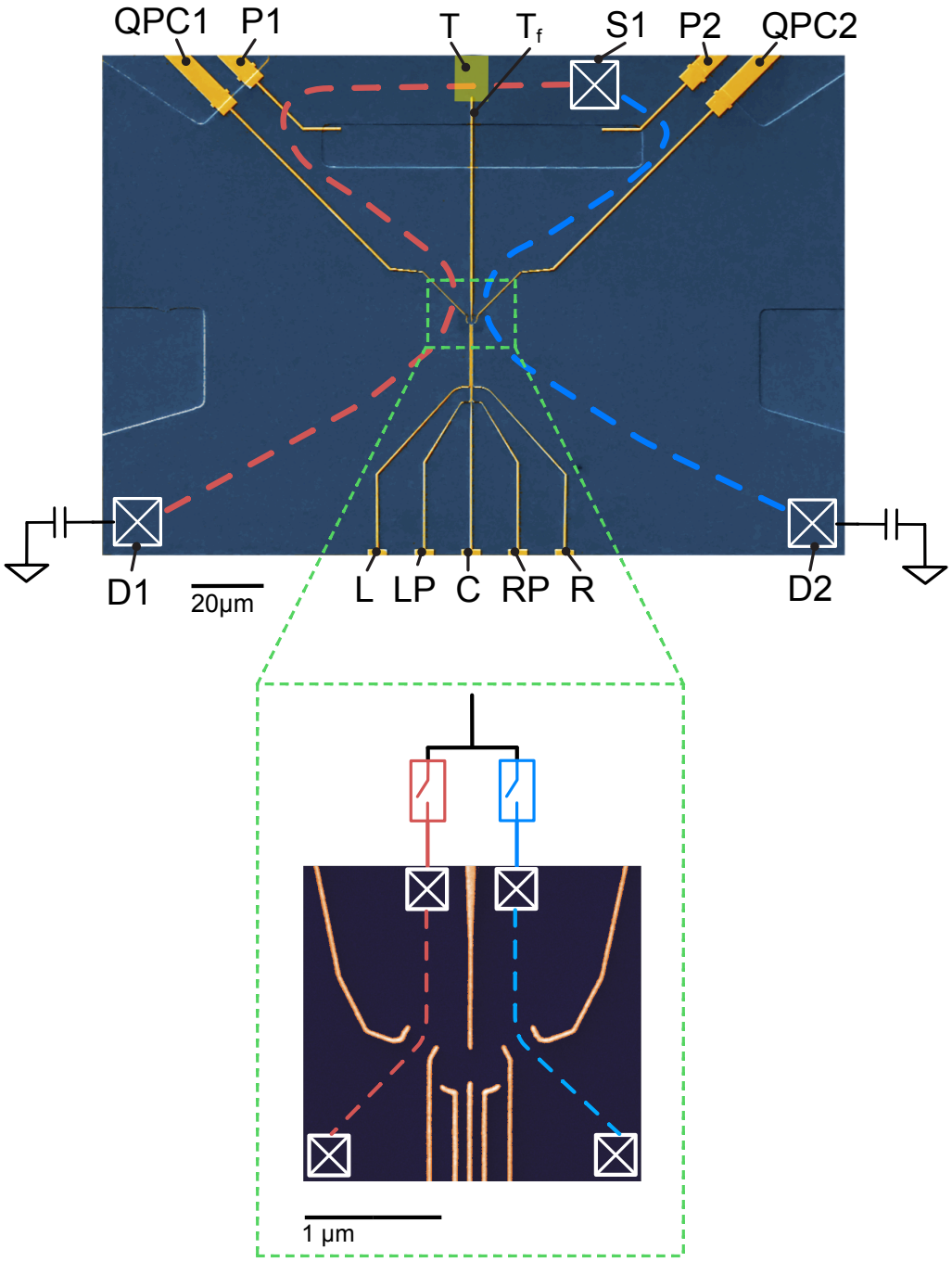

Figure C.2: **Time division multiplexing design.** Scanning electron micrograph of a double dot TDM device. A single source ohmic is present, with current paths controlled by applying an appropriate bias to gates P1 and P2. The area between $P1$ and $P2$ is etched, with no 2DEG underneath. By switching on $P1$ and off $P2$, the quantum state is read through $QPC1$ (red path), whereas switching on $P2$ and $P1$ off, the quantum state is read by $QPC2$ (blue path). Nanosecond switching time allows for successive switching between each QPC measurement round.

Switch Realization

The switches, represented by gates $P1$ and $P2$, in Fig. C.2, control the conduction paths through the quantum point contacts (QPCs). With only a single source ohmic connection, two potential conduction paths are possible via the QPCs. The state of each path is determined by the voltages applied to $P1$ and $P2$. For instance, a sufficiently negative voltage on $P1$ depletes the 2DEG enough to block the conduction path indicated by the red dashed line. Similarly, negative voltage applied to $P2$ blocks the conduction path indicated by the blue dashed line. In this design, explicit path-defining gates are not required since the QPC-defining gates can achieve path control by cutting off conductance through the QPCs. However, it's important to note that in larger-scale designs (see Fig. 6.1), dedicated path-defining gates become essential.

To enable the sharing of a single source ohmic, gate T must be sufficiently elevated above the 2DEG to allow conduction underneath regardless of the bias applied to it. This separation is achieved by placing a 500 nm layer of silicon nitride (SiN) across the entire chip. Specific regions of the SiN layer are etched using a SF6/O2 reactive ion etching process, guided by masking. The 500 nm thickness ensures that gates deposited above the SiN layer do not affect the conductivity of the underlying 2DEG, thus allowing multiple current paths to be defined. All gates except for gate T are deposited before the SiN layer.

One of these etched regions overlaps T and T_f, facilitating electrical connections to define the double dot structure and allowing conduction underneath. After SiN deposition and subsequent etching, gate T is deposited, allowing for electrical connection of T_f to DC sources and conduction under T for our switch realization. Fig. C.3 shows how these two gates are connected, and Fig. 6.1 (d) illustrates a side profile view example of such an etched region.

C.3 Results

The switches are characterized using RF measurements, as depicted in Fig. C.4. In panel (a), the resonant frequency of the device in the double dot regime is investigated as a function of switch status. When measuring through QPC1, the resonant frequency is approximately 287 MHz, with a 3 MHz shift shift observed when measuring through QPC2. Measuring through both QPCs induces an additional frequency shift, though the asymmetry is likely due to slight differences in the tuning of the QPCs, leading to varied resistance values. Conduction underneath T is measured while sweeping the voltage applied, up to -1.75 V. Minimal change in conduction is observed, confirming that the 500 μm SiN barrier is sufficient for isolation.

Next, the closing and opening voltages of the switches are investigated. As suggested in panel

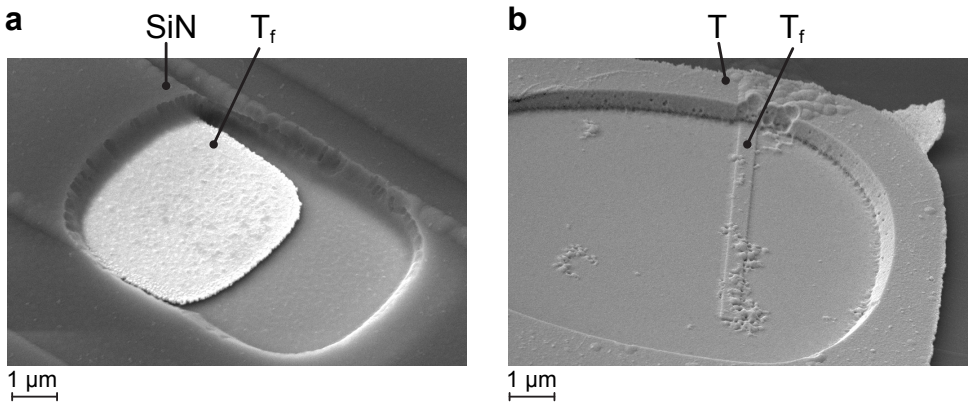

Figure C.3: **Gate connection through SiN layer.** **a**, At the junction of gate T and T_f, corresponding to Fig. C.2. Gate T_f sits underneath the SiN layer, with an etch through to allow for electrical connection. **b**, Alternate design showing gate T deposited after SiN etch, electrically connecting to T_f, but allowing conduction everywhere else under T.

(a), these switches exhibit nearly identical behavior, resulting in similar on and off values for both. Switch $P1$ fully cuts off the channel at -120 mV, whereas switch $P2$ requires a slightly higher voltage, around -175 mV. Both switches allow for full conduction above -100 mV. This outcome is promising, as the required switch voltages are significantly lower compared to typical MOSFET devices, contributing to reduced power dissipation at high switching speeds.

Next, the charge state of the double quantum dot is read out using time division multiplexing through both QPCs. Fig. C.5 (a) illustrates the basic operational principle. One of the wall gates, such as L, is scanned using a sawtooth waveform at 87 Hz, combined with a static DC voltage via a standard voltage combiner. After each scan, a one-dimensional trace of the reflected RF magnitude is obtained through demodulation. Subsequently, switches $P1$ and $P2$ are toggled so that the readout signal from the same scan is detected by the other QPC. Following this, the voltage on the other wall gate (R) is stepped, and the process repeats. This procedure generates two charge stability maps, which ideally should be identical but often exhibit differences due to QPC sensitivity and device characteristics.

To ensure optimal sensitivity for both QPCs, feedback protocols are implemented. Similar to SET feedback detailed in appendix B, the voltages on $QPC1$ and $QPC2$ are adjusted in conjunction with L and R voltages to maintain sensitivity throughout the experiment. However, both tested double dot devices exhibited signs of fabrication defects. Device one (b) had gates that likely leaked to the substrate, resulting in minimal quantization and unintended measurements in a quasi-dispersive regime. In contrast, device two (c) functioned well overall, but sensitivity on $QPC2$ was significantly compromised, likely due to a break in the gate.

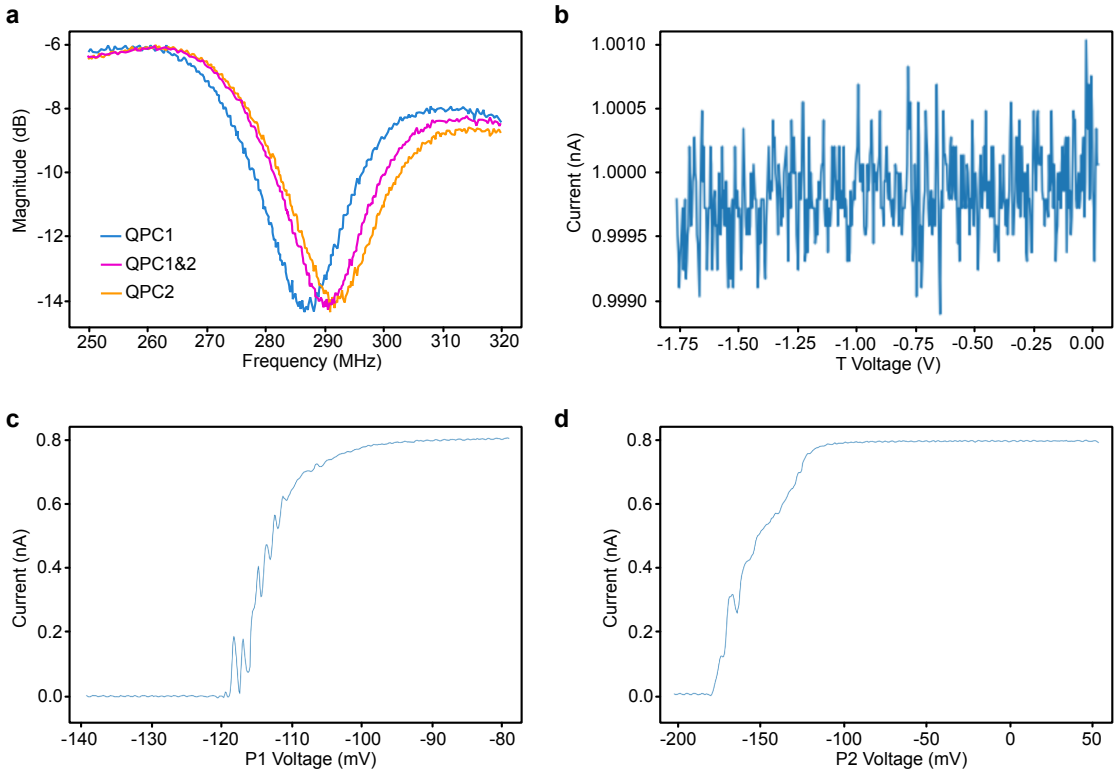

Figure C.4: **Basic operating characteristics.** **a**, Measured RF resonance frequency when using QPC1, QPC2, and both at the same time. The switches are nearly identical, resulting in similar parasitic capacitances and minimal change in the resonant frequency. **b**, Measured conductance under the SiN bridge as a function of T voltage. The T gate can be swept to -1.75 V without a change in conductance, indicating that the separation from the 2DEG is sufficient. **c, d**, Pinchoff characteristics of the two switch gates P1 and P2. Both gates pinch off in a similar manner, fully pinched off below -200 mV and fully open above -100 mV.

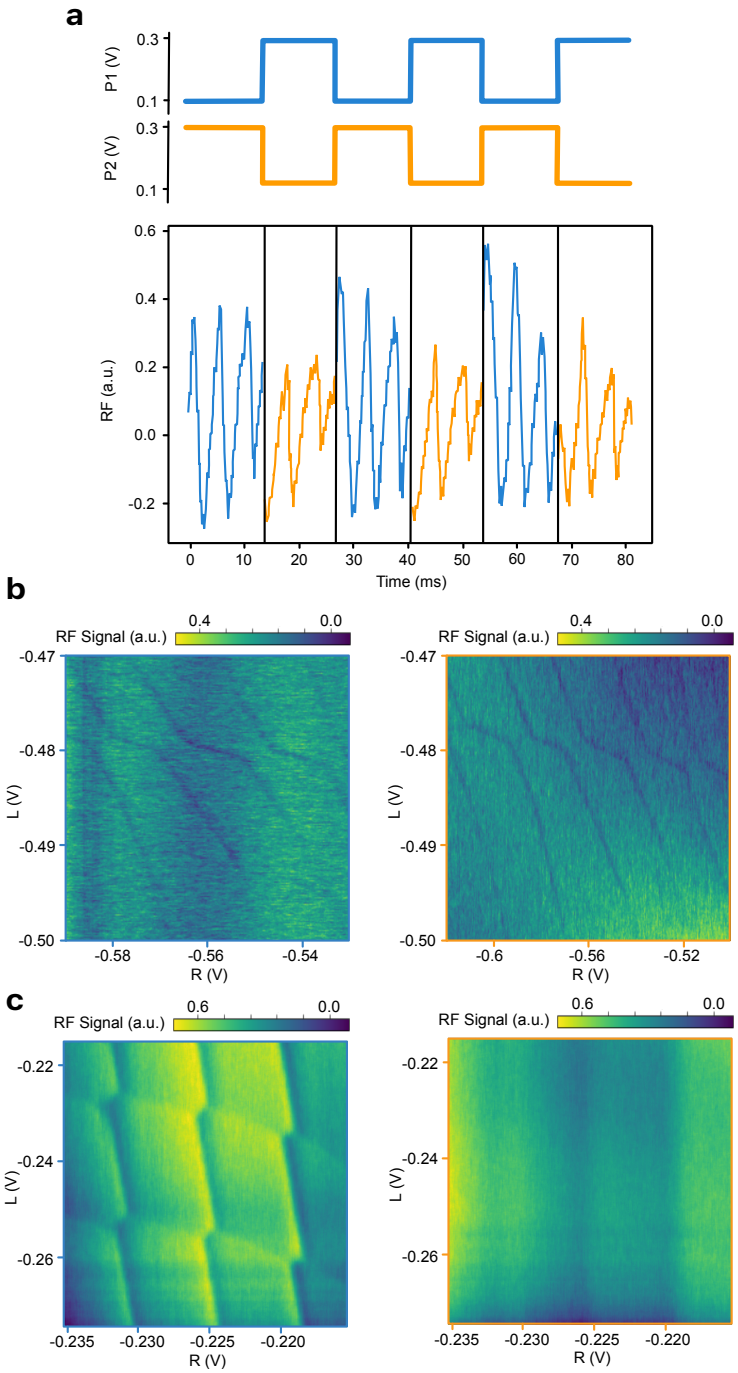

Figure C.5: **TDM Operation.** **a**, Simulation of TDM operation. A gate (for example L) is rastered, providing a single line of data before P1 closes and P2 opens, rastering again for a single line of data measured from the other QPC. **b**, Measured double dot characteristics using a method similar to (a). Unfortunately, device characteristics prevented full characterization and operation in a TDM mode. **c**, Measured double dot characteristics in a second device, using the method described in (a). Here, the outcome is arguably more successful, however a broken QPC resulted in little sensitivity on one half of the device.

C.4 Discussion

The performance limitations of the devices ultimately prevented successful operation in a TDM mode. However, these issues do not invalidate the TDM-like approach itself, as the challenges encountered are primarily inherent to the specific devices rather than the methodology. Future demonstrations, whether in GaAs or Si platforms, can extend to accommodate numerous qubits, potentially eliminating the need for redundant charge sensors for individual quantum dots. In such scenarios, the ability to switch between qubits would become more flexible and contingent upon the behavior of each qubit. For instance, if qubit A is particularly sensitive to interference from qubit B during its operation, it may be advantageous to read out a different, more distant qubit to minimize such interference. Additionally, variations in sensitivity among charge sensors may require sophisticated pulsing sequences aimed at maximizing the signal-to-noise ratio (SNR) of each sensor individually.

One of the biggest gains TDM offers is the shared use of ohmic contacts. Unlike the quantum dots themselves, ohmic contacts are some of the largest features on both GaAs and Si devices, and their shared use among multiple QPCs or SETs represents a huge gain in usable on-chip area. This consolidation allows for more efficient use of the available space, potentially enabling the integration of a greater number of qubits and readout circuits on a single chip. Furthermore, reducing the number of required ohmic contacts can simplify the overall device architecture and potentially improve the reliability and performance of the system. The efficient use of on-chip real estate as well as shared readout chain resources is crucial as quantum processors scale up, making TDM an attractive approach in conjunction with frequency multiplexing for future quantum computing applications.

C.5 Acknowledgements

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Samuel K. Bartee,[1] fabricated and measured the devices, analyzed and presented data, and wrote the manuscript.

M. C. Jarratt,[1] previously started this effort with alternate device designs and characterization that can be found at [299].

Steven J. Waddy,[1] assisted with experimental setup and procedures.

Maja. C. Cassidy,[2] and Geoff. C. Gardner,[3, 4] helped with device design.

Michael J. Manfra,[3, 4, 5, 6] fabricated the 2DEG substrate.

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D

Nanofabrication

Devices in this thesis were fabricated in Sydney University and UNSW research cleanrooms. Each device underwent multiple steps involving resist masking, etching, and metal deposition to create complex structures for the exploration of quantum phenomena. To maximise the chances of a device working (and working well!), fabrication quality and consistency is key. This appendix provides a comprehensive overview of the fabrication processes for GaAs devices (Section D.2) and details each step involved (Section D.1). Due to variations in the capabilities and quality of cleanrooms, some steps may require adaptation to function effectively in different cleanroom settings.

D.1 Process Recipes

Chip Cleaving

The growth of heterostructure materials is a more involved processes compared to generic silicon wafer production. Wafer and batch sizes are small, and conservation efforts must be employed. Typical sample sizes are 5x5 mm, as this is generally adequate to house multiple devices. These chips are usually cleaved manually using diamond-tipped pen. Most III-V materials (in this case GaAs/AlGaAs) have a (100) orientation, which will ultimately aid in the cleaving of chips with straight and perpendicular edges. Safety protocols for cleaving are unique to each cleanroom, as III-V waste is hazardous and has a specialised disposal method.

The location of a cleaved chip relative to the edge of the wafer may impact the performance of the device. For example the edge of the chip may lack a properly grown heterostructure due to the MBE growth process. Logging the location of each cleaved sample will aid in diagnosing any

problems that arise. Redesigning device layout to accommodate for chip shape or defects is not uncommon. To maximize the chances of a successful cleave, the following steps are recommended:

1. Place the wafer next to a metal ruler for stability and proper measurement. Use the grooves of the ruler to make a small incision on the edge of the wafer.

2. Use the cleaving pliers to break off the desired portion of the wafer.

3. Repeat these steps as necessary for the final chip size.

4. Dispose all waste in the proper bins and clean the area of any potential fragments.

Ga Removal

A layer of gallium on the back of the wafer is used for sticking and thermal contact during the MBE growth process. This gallium, if left in place, can contaminate further fabrication processes on the chip and other samples that use the same glassware. The low melting point of Ga makes it easy to remove with an appropriate q-tip. Many of the steps described here, while aiding in Ga removal, are in place to prevent the surface of the chip from being damaged.

1. Place 1-2 drops of PMMA onto a glass slide, and bake at 80 °C until dry.

2. Place an additional drop onto the surface of the chip and place the chip face down onto the dry PMMA.

3. Continue baking at 80°C until the chip is secure (1-2 minutes).

4. The Ga should be soft and easily removable with q-tips. Wipe the Ga away off the backside of the chip, replacing the q-tips as necessary. It is common to use several q-tips during this process. Reheat the chip after every q-tip use.

5. Once the Ga is completely removed, place the chip and glass slide in a beaker of NMP heated to 80°C. Remove the chip from the glass slide.

6. Transfer the chip to a second NMP beaker. The next stage follows directly from here.

Initial Clean

This stage encompasses the most rigorous cleaning of the chip. Contaminants and moisture are removed, ensuring a clean surface for further fabrication. Throughout the fabrication process, further surface damage is likely to occur due to contaminants. It is therefore imperative that the chip is initially cleaned as well as possible.

1. Soak the sample in NMP for 5 minutes at 80 °C. This will dissolve most small organic contaminants.
2. Sonicate the sample in NMP for 2 minutes. Sonicate at a low power, as higher powers can can damage sample surfaces.
3. Transfer sample into a beaker of acetone and let it soak in the acetone for 4 minutes.
4. Sonicate the sample in acetone for 2 minutes.
5. Repeat steps 3 and 4 with the sample in IPA.
6. Bake the sample directly on a hotplate set at 200°C for 5 minutes for complete dehydration.

If more than one chip is being cleaned, it is good practice to clean the chips in separate beakers, as they can damage one another — especially during sonication.

After cleaning, inspect the sample under an optical microscope. Any defects or large damaged sites should be easy to spot, and can potentially harm the performance of the device. Move device patterns as necessary to avoid defects.

Resist Preparation

One of the more technical processes during fabrication involves using resist as a means of protecting the surface. Surface protection is often in the form of a mask, with specific areas exposed for subsequent processes. A resist mask aids primarily in the two critical processes of wet etching and metal deposition. Working with resist involves three separate processes: resist spin, develop, and strip.

Spin

Choosing what resist to use depends on a variety of factors, including desired edge profile, thickness and resolution. Liftoff processes typically require an edge profile undercut, reducing the amount

of connected material aiding in a clean removal of the deposited material. A smooth edge profile is better for etch processes, as the etch follows the resist edge profile, allowing for better continuity of deposited gates. Higher resolution of < 1 μm requires an electron-bean (e-beam) resist, as photolithographic processes (in this clean room) cannot achieve that resolution.

While resists require individualised spin recipes, the overall technique is the same. Before spinning resist, consult data sheets on the particular resists for spin times and resist thicknesses, as well as curing temperatures. Exact spin recipes for a few resists are listed below in Table D.1.

A visual inspection by the naked eye or under the microscope should reveal any contaminants in the resist. These contaminants may not interfere with the patterned areas, but it is best practice to strip the resist and start over.

Several steps remain universal:

1. Place the chip on a clean puck, centering both the puck and chip for minimum vibration during spinning.
2. Dispense an appropriate amount of resist from a pipette onto the chip. The amount you dispense will depend on the size of the chip, resist type and spin recipe. For example, less than one drop of PMMA A3 should be placed on a small (5x5 mm) sample to reduce edge beading.
3. Spin the chip with the desired recipe.
4. Inspect the chip for edge beads and contaminants. If the resist spin is not satisfactory, strip the resist and start again.
5. Bake the chip as appropriate (see Table D.1).
6. Clean the area and return items.

Exposure of a resist is highly dependent on subsequent fabrication steps as well as the particular tools available. A step-by-step guide will likely have few, if any, commonalities due to differences in lithography type, tool model, and calibration. Instead, we move straight to development of a resist once it has been exposed.

Develop

After lithography, the chip is placed in a developer that will dissolve exposed (unexposed) areas of the positive (negative) resist, creating a mask on your sample. Exact develop recipes are listed in Table D.2.

Step	PMMA A3 (100 nm)	PMMA A4 (150 nm)	HMDS (monolayer)	AZ1512 (1 μm)
Spin step	RPM; time (s); acceleration (RPM/s)			
1	1000; 5; 1000	500; 5; 500	3000; 30; 1000	6000; 60; 1000
2	7000; 5; 10000	9000; 5; 4000	0; 0; 1000	0; 0; 1000
3	2000; 50; 10000	4000; 45; 4000		
4	0; 0; 1000	0; 0; 4000		
Bake	time (s); temperature (°C)			
5	60; 180	60; 180	no bake	60; 100

Table D.1: **Spin recipes for a few resists.** All samples will incur some amount of resist edge beading, and the severity of the beading depends both on the size of the chip and the recipe used. Avoiding edge beading during the exposure of a pattern is paramount, as the increased thickness can have unintended consequences of subsequent processes. Many recipes listed here have an edge bead removal (EBR) step, where the chip is spun at a very high rpm for a short period of time.

Resist	PMMA A3	CSAR.09	AZ1512
Solvent; time (s)	MIBK:IPA 1:3; 40	ARP; 30	AZ726; 30
Rinse; time (s)	IPA; 20	IPA; 20	DI Water; 20

Table D.2: **Develop recipes for some e-beam and photo-resists.**

1. Place the chip in the appropriate beaker with the required solvent. Swirl the chip or beaker to ensure constant flow over the dissolving areas. Repeat as required for any subsequent beakers.

2. Dry the sample with a nitrogen blow gun. 10 seconds will completely dry small samples.

3. Bake or plasma ash the chip as appropriate.

4. Clean the area and return items.

Strip

The methods used to strip a resist vary depending on whether the resist has been baked. If not, then dipping the chip in NMP or acetone for 30 seconds will suffice. Baked resist is hardened, and requires a soak in NMP heated to 80°C for 3 minutes and a transfer to IPA for another minute. Make sure the chip is dried thoroughly using a nitrogen blowgun.

D.1.1 Wet Etching

Etching on heterostructure materials removes 2DEG in certain regions, allowing for the definition of novel quantum devices (e.g. Hall bars and Aharonov-Bohm rings) as well as separation of devices on a chip. With similar topology to the much larger geologic structure, this is commonly known as a *mesa etch*.

The continuity of metal gates (often with a thickness less than the etch depth) over an etch boundary necessitate a sloped etch sidewall. This is achieved with the use of a phosphoric acid solution, which isotropically etches GaAs.

1. Postbake your resist after development using the same baking time and temperature as before. This will ensure your resist re-adheres to the surface as it can become slightly detatched.

2. Prepare a 5:1:50 ratio solution of H_3PO_4 : H_2O_2 : H_2O. Make sure the solution is mixed and thermalized. Thermalization may take up to 10 minutes.

3. Place chip in the solution while constantly stirring. The desired etch depth—usually 10 nm below the 2DEG—will determine the time spent in the solution. The solution etches AlGaAs at approximately 2 nm/s.

4. Immediately rinse the chip in DI water for 30 seconds.

5. Strip the resist.

Oxide Deposition

Atomic layer deposition (ALD) is used to insulate gated structures from the surface of the chip, minimising the chance of leakage. This only requires a single tool with no prior preparation (only a clean and dry chip). As growth is entirely tool-dependent, no steps will be provided.

All devices I fabricated in this thesis used Al_2O_3 as the oxide layer, derived from TMA and H_2O. An oxide thickness of $5 - 10$ nm is suitable, requiring approximately 70-150 cycles of TMA at 200 °C. Lower temperatures can negatively affect oxide quality (and imact growth rate), while higher temperatures may affect ohmic contacts.

When thicker oxides are needed ($> 1\ \mu$m), silicon nitride (SiN) is a suitible candidate. Similar to Al_2O_3, deposition of SiN is entirely tool dependent and no steps are provided. A thick photomask is suitable for etching through the SiN layer to the surface in select areas. A mixture of sulfur hexafluoride (SF6) and a trifluoromethane (CHF_3), or purely SF6 within a plasma asher

will etch the SiN layer at a rate of $1 - 5$ nm/s, dependent on flow rate and power. I recommend a layer of Al_2O_3 or metal to serve as the etch stop, to prevent damage to the wafer surface.

Metal Deposition

Metal deposition constitutes multiple steps in the fabrication of a single device. The thickness and kind of metals evaporated onto a chip varies according to the desired outcome, but should always be at most half that of the thickness of the resist for consistent liftoff. Here I cover metallic structures intended for alignment and gating of 2DEG structures. These consist of a TiAu metallic stack, where Ti helps Au adhere to the surface of the chip. Fine features are often in the 40 nm range, at which point the grain structure of the evaporated metal can impact electrical continuity. It is recommended to deposit Au at a rate of 5 Ås^{-1} and Ti at a rate of 2 Ås^{-1}.

1. Spin, expose and develop the appropriate resist.

2. Mount the sample on a silicon wafer in the evaporator. Mounting techniques will differ depending on the proximity of exposed structures to the edges of the chip. In general, very thin pieces of polyimide tape and a steady hand should suffice for most samples.

3. Evaporate the metals according to desired outcome and specific tool procedures.

4. After removal, place the chip into NMP heated to 80 °C. For thinner metal depositions and resists, leave the sample in for no more than 30 minutes. Thicker resists may require up to 1 hour. Significantly longer liftoff times may result in the metal resettling on the surface of the chip in undesirable locations.

5. Sonicate the chip in low power in 5 to 10 s intervals. Smaller features are especially delicate and longer sonication times risk damaging or removing them. With visual inspection, repeat sonication as necessary until liftoff is complete.

6. Place the chip in IPA for 5 minutes.

7. Remove and dry chip.

The deposition and annealing of ohmic contacts is covered more extensively in appendix E.

D.2 Example Recipe

An example recipe for a GaAs chip, which includes hall bars, gated structures and ohmic contacts is detailed below.

1. **Cleave and clean:** Sec. D.1, D.1, D.1
2. **Metal deposition:** deposit TiAu alignment markers. Sec. D.1, D.1.1
3. **Mesa etch:** etch away all undesired 2DEG regions. Sec. D.1, D.1.1
4. **Ohmic contacts:** deposit ohmic contacts and anneal. Sec D.1, appendix E
5. **Oxide deposition:** Al_2O_3 oxide layer. Sec. D.1.1
6. **Metal deposition:** deposit gated structures. Depending on the design, this may be broken into multiple steps. Sec. D.1, D.1.1

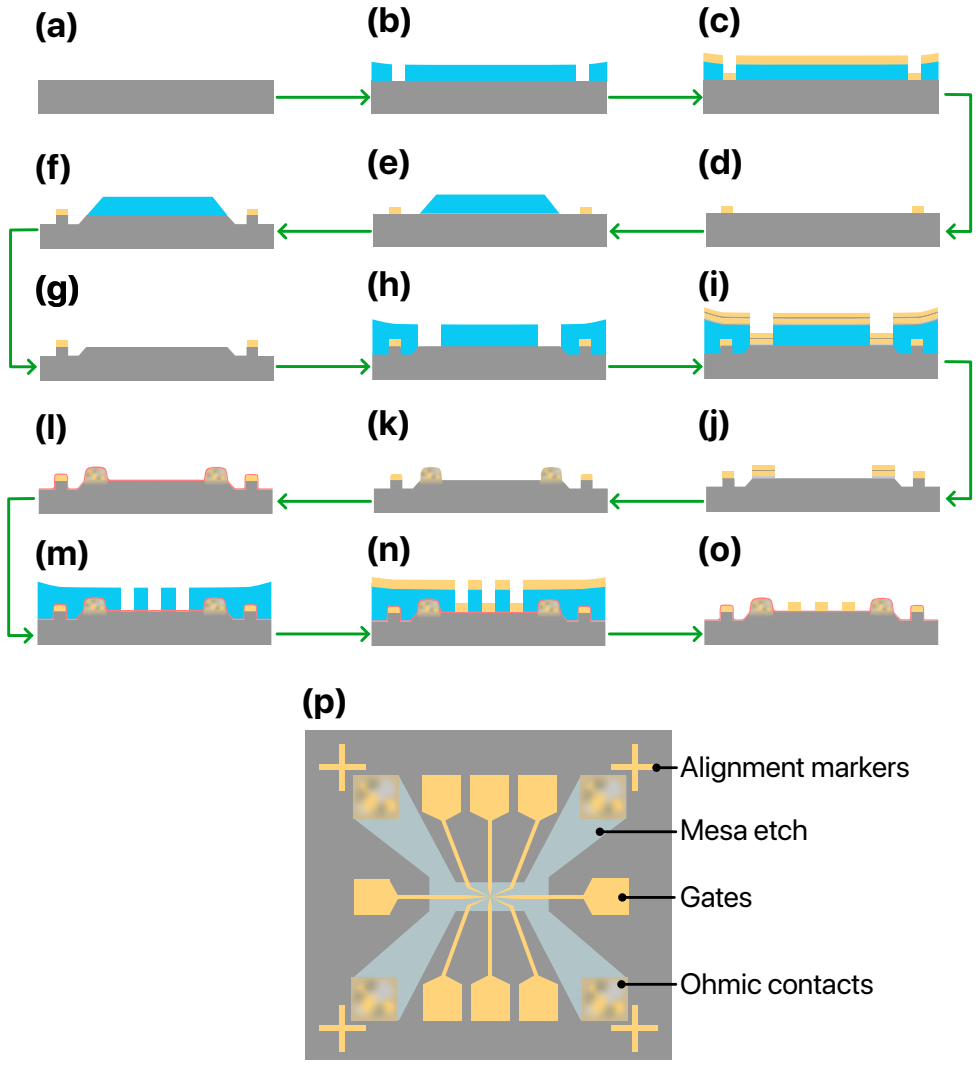

Figure D.1: **Side profiles of an example fabrication process flow.** (a)-(o) A flow chart of the fabrication steps involved in a typical device. (a)-(d) Cross section of alignment marker placement starting with (a) cleaning the sample, (b) spin coating and exposing the resist, (c) evaporating Au onto the surface and (d) liftoff. (e)-(g) Mesa etch consisting of resist mask (e), etching (f) and resist removal (g). (h)-(k) Evaporation and annealing of ohmics. (l) A thin Al_2O_3 layer is deposited on the surface to prevent gate electrodes from leaking to the 2DEG. (m)-(o) These gate electrodes are deposited with similar methods to the alignment markers. (p) A cartoon of a fully completed device, with all components created with the corresponding to steps (a)-(o) labelled.

E

Analysis of GaAs Ohmic Contact Behavior

All devices presented in this thesis possess ohmic contacts. These are electrical connections to the outside world that serve as an electron reservoir, cross-device (source-drain) bias, and grounding for RF-based operations. The performance characteristics of ohmic contacts (referred to as "ohmics") fundamentally influence the behavior of a device and often play a decisive role in the success or failure of an experiment. It is therefore imperative not only to understand how to consistently fabricate functional ohmics but also to accurately diagnose issues with those that do not perform as intended.

In this section, I exclusively address ohmic contacts for GaAs heterostructures. Unlike other systems such as silicon or indium arsenide (InAs), establishing a reliable electrical connection to a GaAs-based 2DEG involves complex and unconventional fabrication techniques that are that are highly sensitive to environmental variations. The distinction between a functional and defective ohmic contact, irrespective of the fabrication recipe, often hinges on minute details that are frequently overlooked.

Ohmic contacts for GaAs devices have a rich historical background, and their underlying mechanisms have been extensively documented in literature spanning over six decades [300]. A full description of their inner workings is beyond the scope of this thesis, instead I offer a short overview of ohmic contact behaviour and pertinent fabrication processes. I also address specific fabrication challenges that can lead to suboptimal ohmic performance. Finally, I present an analysis of ohmic contact performance across multiple failed and successful devices fabricated during the course of

my PhD.

E.1 Theory

The most common way of electrically connecting to a 2DEG in GaAs is though diffusion of a metal or alloy from the surface to the heterojuction underneath [301]. Various techniques exist for achieving this, and here, I employ a widely-used approach of depositing a specific NiGeAuNiAu layer onto the chip's surface, followed by high-temperature annealing for diffusion. In this layer stack, the 67-33 Ge-Au (weight %) composition forms a eutectic alloy. Melting at $361°C$, the alloy penetrates through the GaAs surface and serves as the primary doping agent for conduction [302]. The bottom Ni layer is typically very thin, not exceeding more than 50 Å in any device fabricated here. It serves multiple rolls, acting as a wetting agent preventing the Ge-Au from balling up, reducing surface oxides, and acilitating the formation of further compounds within the GaAs layers. The formation and interaction behaviour of these compounds is complex and dependent on both the composition of the deposited layers, and the annealing time and temperature [303]. Some of these binary and ternary compounds, such as $\beta-$AuGa and NiAs (containing small amounts of Ge) are shown to contribute to electrical connectivity, whereas others like NiGe have more adverse effects [304].

The conduction mechanism of the ohmic contact can be described by one of three models: thermionic emission (TE), thermionic field emission (TFE) and field emission (FE) [305–307]. These mechanisms are contingent upon the temperature of the system as well as the doping level (i.e., the extent of diffusion) in the 2DEG. Higher doping levels lower the Schottky barrier ψ_B of the metal-semiconductor interface, particularly at lower temperatures, leading to the dominance of the FE conduction model [308]. Conversely, at lighter doping and lower temperatures, the TFE or TE conduction models may fail to overcome ψ_B, resulting in near-infinite resistance for the ohmic contact. At these low temperatures, the extrinsic nature of the semiconductor leads to electron freeze-out [309]. TE conduction predominates at high temperatures, explaining why almost all ohmic contacts—regardless of their functionality—conduct at room temperature and in well-lit environments.

The resistance of ohmics as a function of temperature is not directly measured here. Instead, both the resistance of ohmic contacts and that of the 2DEG are reported. It's important to recognize that ohmic and 2DEG resistances exhibit distinct behaviors over the same temperature range. Due to some thermionic emission at higher temperatures, ohmic resistance generally increases as temperature decreases. The quality of the ohmic determines how much this resistance changes.

In contrast, 2DEG resistivity experiences the opposite effect, decreasing significantly at lower temperatures as the sample's mobility increases [310, 311]. In certain samples, the resistance may appear to decrease with temperature before sharply increasing to open-circuit values, reflecting the competing changes in 2DEG and ohmic resistance.

E.2 Fabrication

After deposition (see Appendix D for details), ohmics are annealed in an oven with a continuous flow of forming gas (96% Ni, 4% H). The time and temperature of the annealing process significantly influence the resistance outcomes of the ohmic contacts, owing to the formation and interaction of various compounds during diffusion [312]. The optimal time and temperature for as-deposited ohmics with our particular composition is $450°C$ for 140 seconds (although larger samples may require slightly longer annealing times), in broad agreement with the conclusions of other experiments [302, 303]. The poor controllability and considerable sensitivity to the environment make ohmic contacts one of the least consistent components of device fabrication. Contributing factors to poor performance can be categorized into three main areas: evaporation, annealing, and 2DEG destruction.

Evaporation

Each layer of an ohmic stack is deposited using an electron-beam evaporator. Hysteresis in calibration or equipment malfunction can cause variations in the evaporation rate and final thickness from the specified parameters, thereby impacting the ultimate outcome of an ohmic contact. These problems are sometimes visually spotted, such as in Fig. E.1 where slow evaporation of gold and interaction with the photoresist AZ1512-HS leads to a bubbling effect and poor adhesion to the previous metallic layer. In other cases, the problems may only be revealed once the ohmic is annealed.

A working annealed ohmic has a specific look and grain structure, and deviations from this likely indicate further performance problems. While a 'good-looking' ohmic does not necessarily indicate performance, it does help eliminate certain issues when diagnosing what potentially went wrong. These problems are rare and easy to correct. A full table detailing ohmic performance in particular environments is detailed in table E.1.

The Annealing Process

Another, more common subset of problems involves the annealing process directly. Ohmic contacts are expected to function within a specific range of time and temperature during annealing. While this range can be relatively generous, it's possible to under- or over-anneal a sample, resulting in certain characteristic behaviors. Other issues may arise due to inadequate cleaning before deposition and/or annealing, leading to burnt ohmic contacts, as well as changes in the annealing atmosphere—all of which are visually distinct and identifiable.

An under-annealed ohmic occurs when the time and temperature are insufficient to establish a FE electrical connection to the 2DEG. In the most extreme example, un-annealed ohmics may have very slight conduction between one another in a well-lit, room temperature environment as electrons are in a sufficiently excited state to overcome the Schottky barrier. Dim the environment and this conduction is expected to decrease, to the point of open circuit behavior. Under-annealed ohmic contacts typically display significantly lower conductivity at room temperature (under light) compared to properly functioning ohmic contacts. The time needed to fully anneal a small test sample (approximately 2×2 mm) is often less than a larger typical 6×6 mm chip containing multiple devices.

Over-annealed ohmics exhibit similar behaviour. Using excessively high temperatures for prolonged periods transforms NiAs compounds into NiGe compounds and alters $\beta-$AuGa into $\alpha-$AuGa, resulting in a different crystalline structure [313, 314]. Conduction through these altered structures can vary significantly depending on the diffusion of the compounds. In well-lit, room temperature environments the behaviour of these ohmics can be indistinguishable from working ones. This conduction is significantly reduced in a darker environment and disappears entirely at lower temperatures. Both under- and over-annealed ohmics have different visual characteristics to working ohmics (typically smaller and larger grain size respectively), but can sometimes be hard to distinguish when the annealing characteristics separating working and non-working ohmics are small.

A perfect anneal is meaningless if the ohmics themselves aren't adequately cleaned. Cleaning must occur both before and after deposition, as residues such as resist or other organic material left behind can burn and damage the ohmic contacts. Burning on top of the ohmics, depending on its severity, decreases performance to the point of open-circuit behaviour. The 50 nm Au capping layer can help shield the more critical diffusion layers from damage if the burning is localised. Burning occuring underneath the ohmic, has always resulted in open-circuit behaviour. This type of burning is much more catastrophic to the diffusion process, and even in visually-localised areas impacts the ohmic performance as a whole.

Lastly, an inadequate forming-gas atmosphere will almost certainly lead to broken ohmics. The absence of a forming gas can result in oxidation, negatively impacting diffusion. Their behaviour is often open-circuit in cold environments, and visually are very easy to distinguish from those subjected to proper annealing methods.

2DEG Destruction

It should be immediately obvious that even if diffusion of metallic compounds down to the 2DEG is successful, absence or removal of the 2DEG between any two particular ohmics will render them useless. 2DEG can be inadvertently removed or damaged by other fabrication processes. In all cases, this leads to open-circuit behaviour.

The most common way a 2DEG is removed is through an etching process. In the complete fabrication recipe D.2, two separate etch processes are used, which can have different effects on the 2DEG. Removal of the accumulated surface oxide layer with HCl before ohmic deposition is unlikely to damage the 2DEG unless the etch lasts too long. The thick photoresist layer, combined with the slow etching rate of $\sim 0.3\ \mathrm{nm\,s^{-1}}$ means that the only 2DEG likely to be removed is that directly below the ohmics themselves. Etching large areas of the mesa with a dilute H_3PO_4 solution (D.1.1) is more likely to cause problems. Not only does the solution etch at a much faster rate ($\sim 1.6\ \mathrm{nm\,s^{-1}}$), but it is more likely to penetrate through and etch underneath e-beam resist layers acting as a mask. These effects may not be immediately obvious visually, however looking at both surface roughness and visual characteristics under a scanning electron microscope will reveal the extent of the problem. This is remedied through using a thicker e-beam resist layer and using a monolayer primer to help the resist stick to the surface of the chip.

Physical bombardment of the chip via dry plasma etching processes can also damage the 2DEG. An argon mill, even for a short period of time, is likely to etch away at the surface and significantly increase surface roughness, and is best avoided unless critically needed. Similarly, a reactive ion oxygen plasma etch can damage the 2DEG to the point of open circuit behaviour under certain conditions. It is better in this case to use a plasma asher for cleaning the surface of the chip. Issues caused by these processes are relatively simple to diagnose and change.

In some cases, the problem may not reside with poor ohmic annealing or 2DEG destruction, instead originating from a complete absence of a 2DEG. The epitaxially grown wafers, while generally consistent, face similar fabrication issues encountered by any other research-based fabrication process. The small-scale, custom nature means unexpected problems in growth may arise. A more common and systematic issue is present at the edge of these wafers. Due to their growth process, inconsistencies or absences in certain layers will occur near the outer edge of all GaAs (and other

Ohmic Type	Light, 300 K (Ωcm^2)	Dark, 300 K (Ωcm^2)	4 K (Ωcm^2)
Ideal	0.1	$0.1 - 0.13$	$10^{-6} - 10^{-2}$
Over-Annealed	0.1	$0.2 - \infty$	∞
Under-Annealed	$0.5 - 10$	$10 - \infty$	∞
Underside Burn	$0.5 - 10$	∞	∞
Overside Burn	$0.1 - 10$	$0.1 - \infty$	$10^{-2} - \infty$
No Atmosphere	$2 - 50$	∞	N/A
Incorrect Material	∞	∞	N/A
Destroyed 2DEG	$0.1 - \infty$	∞	∞

Table E.1: **Performance of a working ohmic and non-working ohmics.** Understanding the characteristics of a broken ohmic may lead to understanding of what is causing it to underperform.

epitaxially grown) 2DEG materials. An ohmic may not work simply because it is too close to the edge where the GaAs/AlGaAs heterojunction layer is poorly defined.

Finally, like any electrical circuit, too much power through an ohmic pair will break them. The amount of power depends on factors such as the size of the ohmics, 2DEG material and conduction area, and temperature. In most cases, this power is well above that required to drive unnecessary quantum transitions and substantially heats the system. It is prudent when testing any ohmics to make sure they are not breaking due to poor forethought of the power an ohmic can withstand.

E.3 Performance

I classify ohmic performance as binary. Either resistance at mK temperatures is low enabling device characterisation, or is open circuit-like, preventing further experimentation. In this section, I detail the performance and characteristics of several working and non-working ohmics, and discuss certain features that can to quickly determine the viability of a device.

The very best ohmics quoted in literature have a contact resistance of 10^{-6} Ωcm^2 for similar n-type GaAs heterostructures and ohmic stack materials [302]. The best ohmics I have personally fabricated have a contact resistance of 10^{-4} Ωcm^2. While this value is higher, it still translates to approximately $\sim 100\,\Omega$ per ohmic, much smaller than the in-line resistance added by some cryogenic device motherboards, dc filtering present in the fridges and characteristic quantized resistance.

The viability of an ohmic can only be established at the base temperature of the device in question. There are some immediate indicating factors, such as open-circuit behaviour in a light or dark environment (see Table E.1) and immediately increasing resistance with a lowering temperature (Fig. E.2 (b)), which almost certainly result in open-circuit behaviour. When an ohmic conducts

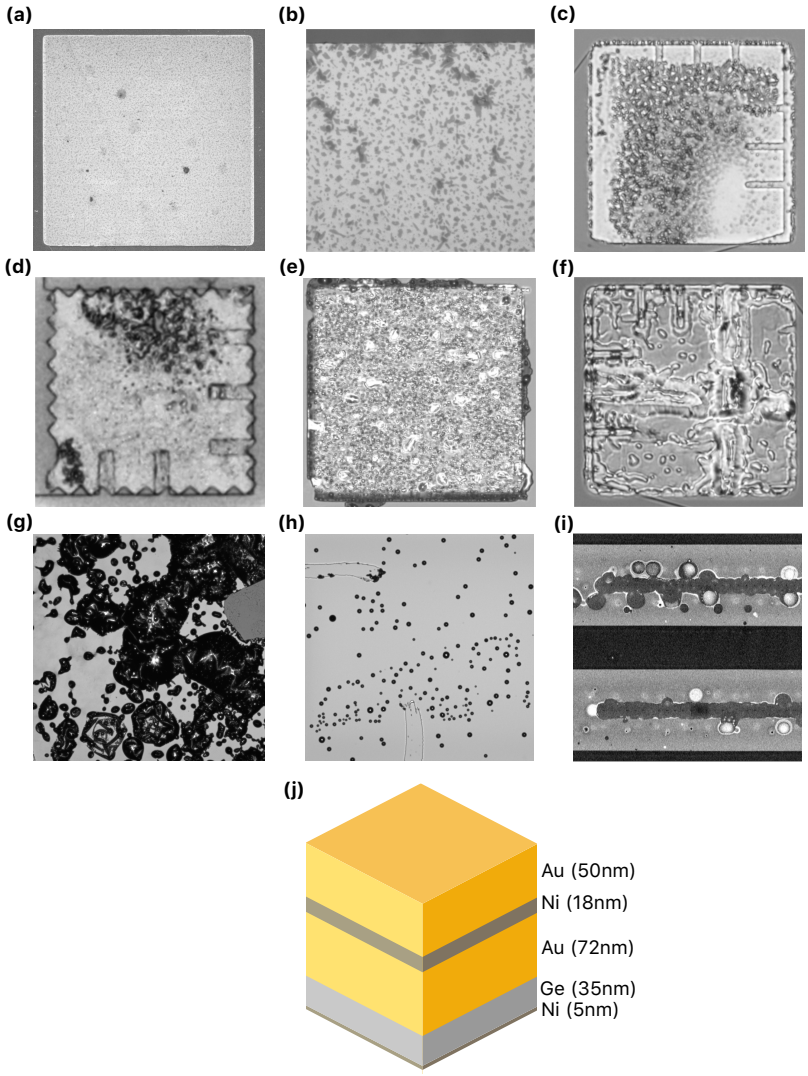

Figure E.1: **Visual examples of working and broken ohmics.** **a**, A working ohmic with resistance 10^{-4} Ωcm^{-2}. This specific ohmic was annealed at $450°\text{C}$ for 140s. **b**, Characteristic features of an over-annealed ohmic ($450°\text{C}$ for 300s). The grain structure is significantly larger. **c**, Annealed ohmic with surface burns that may affect performance. **d**, Annealed ohmic with an unknown material (likely resist) that burned underneath. **e**, Annealed ohmic with unknown material properties. The evaporated stack of material likely deviated significantly from what is specified in (j). **f**, Annealed ohmic without the forming gas atmosphere, leading to oxidation during the annealing process. **g**, Bubbling and separation of the gold layer from the material underneath after bad evaporation. **h**, Similar to (g), the gold here still exhibits some bubbling but is reduced. This is still likely to affect ohmic performance once annealed. **i**, Undesired etching of the GaAs wafer. The lighter, unetched areas should be monotone, however the etchant has penetrated through the etch mask, affecting the surface and 2DEG underneath. **j**, Typical ohmic material stack used to create ohmics with desirable characteristics.

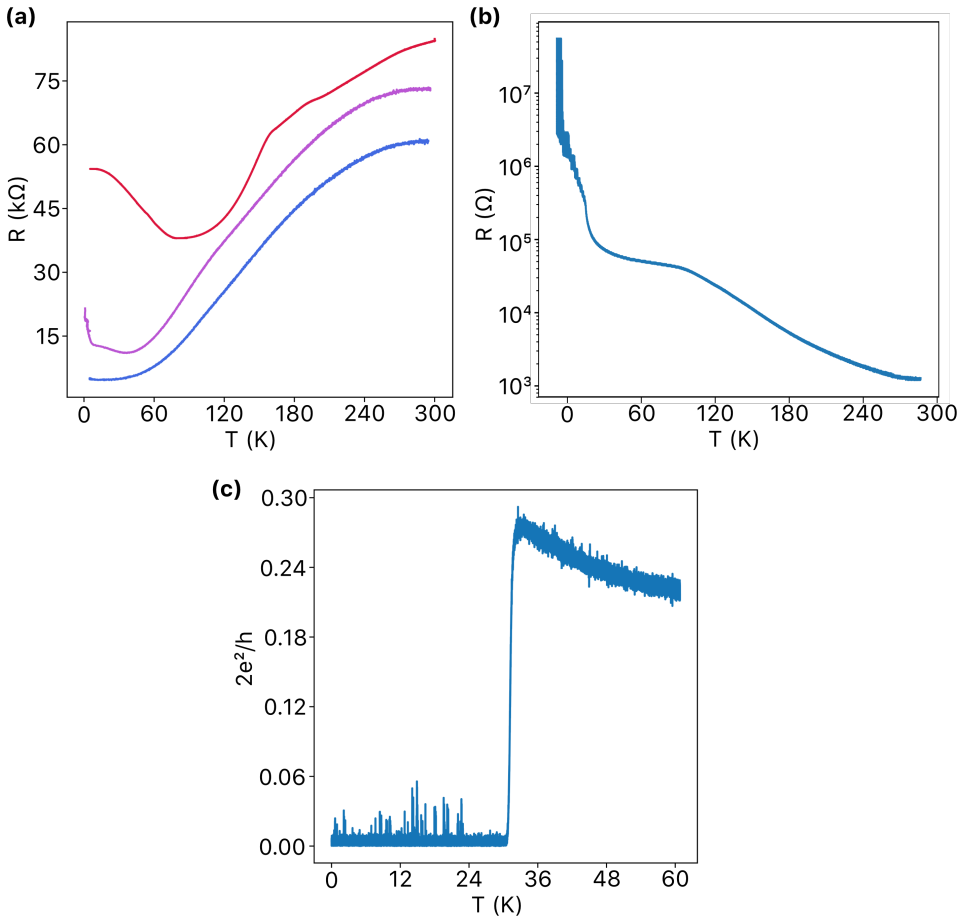

Figure E.2: **Ohmic resistances as a function of temperature.** **a**, Resistance of ohmics (and 2DEG) vs. temperature behaviour of three ohmic pairs fabricated separately. The blue line shows the best and most typical behaviour, with the resistance falling in the characteristic 'S' shape as mobility increases with lower temperatures. The purple line shows an ohmic pair which increases in resistance at very low temperatures, and the red an ohmic pair which starts increasing in resistance at $\sim$ 70 K. $70-80$ K is typically where sub-optimal ohmics increase in resistance, as electrons conducting via TE and TFE become frozen out. **b**, Resistance of ohmics vs. temperature for a pair of over-annealed ohmics. Here, TE is the dominating conduction model and as temperatures lower, resistance increases substantially to functionally open-circuit values. **c**, An LED-shocked 2DEG, depleted of electrons, regains the electrons via TE and TFE as temperature is slowly increased.

via a TFE mechanism, however, these issues may not emerge until lower temperatures are reached. Fig. E.2 (a) shows this behaviour, where some ohmics may increase in resistance at lower temperatures after an initial decrease. These ohmics, while not ideal, work at low temperatures, but this is not always true. Once an ohmic cools past $\sim$ 77 K, a point at which electrons transmitted via TFE freeze out, it is very likely that the ohmic will work. There are instances, however, where I have encountered an ohmic very suddenly behaving in an open-circuit fashion below 4 K.

Not every ohmic that appears broken actually is broken, as completely depleting the 2DEG of electrons is possible. 2DEG depletion can be achieved through a large voltage spike on gates (this can lead to gates breaking), or through exposure to a light source. Fig. E.2 (c) in particular is an ohmic pair exposed to a white, low power LED at its activation voltage for less than one second. At base temperature, conduction immediately ceases with exposure. The 2DEG quickly repopulates as temperature rises.

E.4 Conclusion

Ohmic contacts represent some of the most challenging and least consistent aspects of fabricating quantum devices. Their extreme environmental sensitivity coupled with complex fabrication techniques mean they are often prone to failure. There are other ways of connecting to the 2DEG that are arguably more reliable, such as ion implantation [302, 315]. InAs and silicon ohmics are even easier; the 2DEG, only $\sim$ 10 nm below the surface in some cases, can electrically connect to a deposited metallic pad with no annealing required. Despite all these factors, ohmics will not be supplanted by a superior technology any time soon. The relative ease of fabrication and design flexibility of ohmics, as well as GaAs characteristics all mean these systems are very well suited to small-scale research applications. Many breakthroughs in quantum systems have used ohmics, and I believe there are still many to follow.

F

Setup and Operation of Cryogenic Systems

The operation of Si and GaAs qubits is only possible at extremely low temperatures. Achieving this is a feat in itself, as temperatures of 10 mK and pressures of 10^{-9} bar–while accommodating for high frequency control of sensitive quantum devices–are prerequisites before most quantum operations can begin. Interestingly, the cooling technology primarily draws from simple compressor and pump solutions that have been in existence for over a century. What distinguishes cryogenic dilution refrigerators from their household counterparts is the innovative and advanced implementation of these technologies. The following Appendix details the fundamental principles behind the dilution fridge.

Temperature

Cooling to 4 K is easy. In a BlueFors LD-400 (the one principally used in this thesis), the physics of getting to 4 K are almost exactly the same as your freezer achieving 263 K, primarily involving a compressor and insulation. In this setup, a pulsed-tube Cryomech compressor combined with a vacuum chamber and radiation shield (for effective thermal design) suffice. Many quantum systems can be screened at this temperature, and their behaviour is *good enough* to understand some of the quantum behavior. The thermal energy often exceeds the energy splitting of qubits, however, introducing significantly more noise and necessitating even lower temperatures for qubit control.

Cooling to 10 mK is hard(er) and introduces some novel physics. These temperatures are

reached by using a dilution circuit of condensed ^{3}He and ^{4}He. The process begins with the liquefaction of ^{3}He and ^{4}He alone, which leads to reaching 1 K by leveraging evaporative cooling effects at extremely low pressures. At approximately 0.8 K, the ^{3}He and ^{4}He phases separate, forming an almost-pure ^{3}He layer atop a denser ^{4}He-rich phase. ^{3}He atoms have a larger zero-point motion and occupy a larger space due to their lower mass [316]. Consequently, the binding energy between ^{3}He atoms is smaller than that between ^{4}He atoms, prompting a preferential movement of ^{3}He atoms into the ^{4}He phase to maximize their binding energy. The Pauli exclusion principle prevents the complete mixture of the two phases, instead settling in the ^{4}He-rich phase at approximately 6.6%. The higher vapor pressure of ^{3}He is useful for cooling, as it can be preferentially removed by pumping. Osmotic pressure within the circuit causes ^{3}He to migrate upward through the ^{4}He phase, constituting the primary source of cooling at these ultra-low temperatures. These phases are temperature separated, with the ^{4}He-rich phase at the mixing chamber (10 mK) and the ^{3}He-rich phase at the still (800 mK) (see Fig. F.1) [317]. Adding heat to the still increases vapor pressure, increasing circulation, improving cooling power, and lowering base temperature.

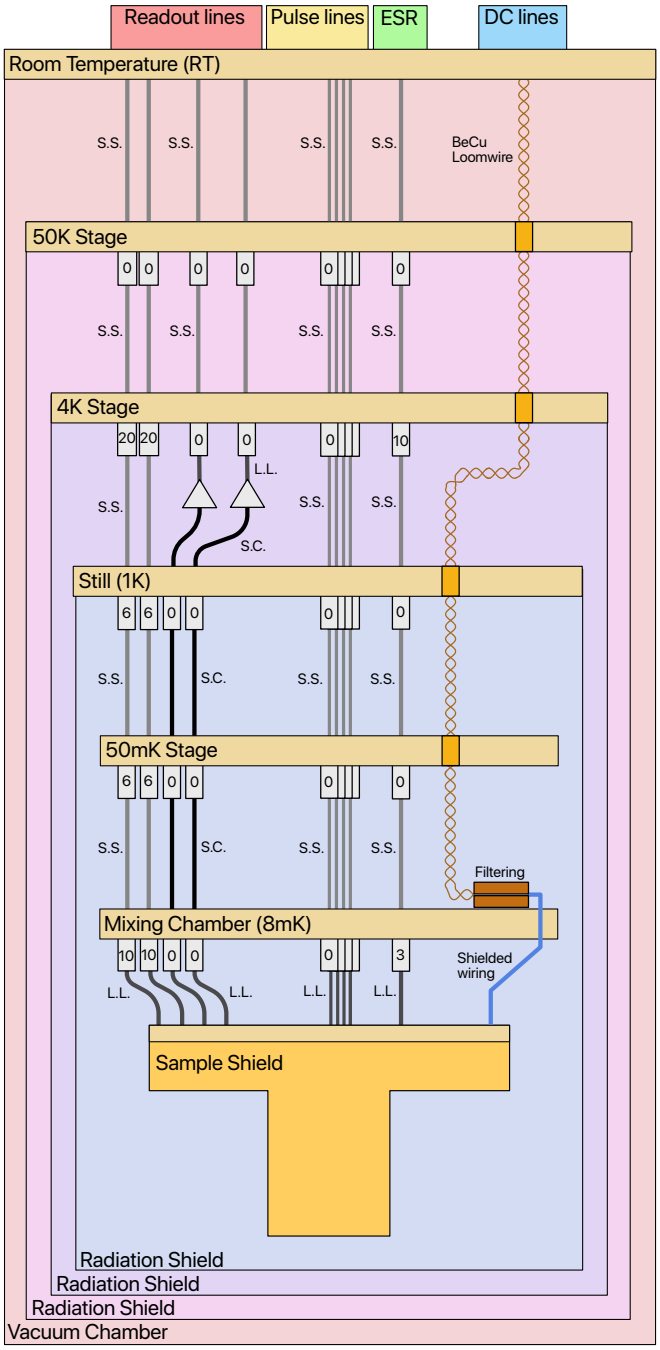

Figure F.1: **Internal layout of a cryogenic fridge.** A typical internal fridge setup, closely resembling the actual experiment performed in Chapter 5. Stainless steel (S.S.) coaxial lines are used for both transmission readout lines, pulse and the ESR lines. Superconducting (S.C.) lines help reduce any losses on signal reflection for readout, and low loss (L.L.) lines are used exclusively below the mixing chamber due to their flexibility and ease of incorporation into tight spaces. DC lines are filtered at the mixing chamber.

DC Signals

The majority of signals received by a device are DC. It is imperative that the initial noise on these lines is as low as possible, and any noise present is further attenuated by thermalization/filtering within the fridge. For all experiments conducted in this thesis, the DC source is the "MDAC", a multi-channel DC signal source designed and built by Steven Waddy in-house [318]. It is capable of providing 64 channels of long-term stable, low noise ($7.5\ nV/\sqrt{Hz}$) 20-Bit signals, suitable for both negative-voltage GaAs-gate and positive voltage Si-gate devices. The significance of high-quality signals cannot be overstated: low-quality signals lead to low-quality data. The DC signals sourced from the MDAC are connected directly to a breakout box which allows individual line-switching between ground, DAC, floating, and common bus channels. From here they connect to the fridge via a shielded Fisher circular connector. Inside the fridge, DC signals are directed down 24 twisted pairs of BeCu loom wire that is thermalized at each temperature stage for extremely low (< 1 ohm) resistance at cryogenic temperatures. Filtering takes place at the mixing chamber and comprises three components: LC, RC, and sapphire stripline filtering. target high-frequency noise, with cutoff frequencies of 80 MHz and 70 kHz, respectively, while the stripline filter reduces electron temperature through meander thermalization.

High Frequency Signals

High frequency pulsing signals require coaxial cables, as they cannot be transmitted down DC lines without incurring high levels of loss. The RC time constants of the DC loom wire–even without filtering–are too long, causing signal distortion and impedance mismatch. The coaxial lines, instead, are impedance matched to $50\ \Omega$ and are rated well past 10 GHz in many cases. In Fig. F.1, pulsing and readout lines labelled 'S.S.' are semi-rigid SCuNi-CuNi coaxial lines of model number BlueFors BF0030235. These are capable of up to 18 GHz, well past the resonance frequencies of spin qubits and pulsing requirements for control. Stainless steel is chosen as a compromise between low thermal conductivity and acceptable loss levels. In instances where thermal isolation between plates is unnecessary and more flexible lines are required for confined spaces, low-loss (L.L.) 0.086 inch tin-plated aluminium (S086MMAL, rf-coax) lines often often suffice. The 0.086 inch SS-BeCu coaxial line from rf-coax is is used for the high frequency microwave signals and is rated to 27 GHz (S086MMSB). Coaxial lines with higher frequency ratings require special-purpose connectors rather than the standard SMA connector. To preserve signal integrity, readout lines must exhibit minimal loss. Hence, to minimize attenuation, superconducting (S.C.) NbTi-NbTi lines

are employed for the reflected RF signal. These are particularly fragile and are prone to breaking solely at cryogenic temperatures. Attenuators are used on every cooling stage of every RF line. Even when no attenuation is required, 0 dB attenuators help to thermalize the inner core of these lines, lowering the noise temperature.

High frequency readout signals are amplified by a HEMT cryogenic amplifier placed at the 4 K stage of the fridge. These provide approximately 40 dB of signal gain, with a noise temperature of $\sim$ 3.5 K. At low frequencies ($<$ 250 MHz) CITLF1 amplifiers from Cosmic Microwave are preferred, and above this we use amplifiers from Low Noise Factory.

Thermal Considerations

At deep cryogenic temperatures, cooling power is on the order 10 μW. Such low cooling power means device thermalization and power dissipation must be considered during experimentation. For example, in Chapter 5, poor thermalization to the mixing chamber plate, as well as a proximally placed cryo-CMOS controller meant electron temperatures approached 1 K while the mixing chamber maintained a temperature of 20 mK. Very subtle changes in the environment and cold finger properties can result in drastic changes in temperature. Samples with a ramping magnetic field are expected to increase in sample temperature (observed up to 300 mK) due to eddy-current-induced heating effects.

As an exercise, especially poor thermalization was explored by Steven Waddy, and a sample temperature of 60 K was achieved (with heating) while inside a superconducting magnet at 7 T.[1] If temperatures even close to the reported mixing chamber temperature are desired, considerable thermal anchoring is a requirement.

[1] He was investigating the classical properties of the Hall effect in GaAs, and required especially elevated temperatures to understand some characteristics of the 2DEG.

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